CPLD Libraries Guide

UG606 (v 12.3) September 21, 2010

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About this Guide

This schematic guide is part of the ISE documentation collection. A separate version of this guide is available if you prefer to work with HDL.

This guide contains the following:

- Introduction.
- A list of design elements supported in this architecture, organized by functional categories.
- Individual descriptions of each available primitive.

About Design Elements

This version of the Libraries Guide describes design elements available for this architecture. There are several categories of design elements:

- **Primitives -** The simplest design elements in the Xilinx libraries. Primitives are the design element "atoms." Examples of Xilinx primitives are the simple buffer, BUF, and the D flip-flop with clock enable and clear, FDCE.
- **Macros -** The design element "molecules" of the Xilinx libraries. Macros can be created from the design element primitives or macros. For example, the FD4CE flip-flop macro is a composite of 4 FDCE primitives.

Xilinx maintains software libraries with hundreds of functional design elements (macros and primitives) for different device architectures. New functional elements are assembled with each release of development system software. This guide is one in a series of architecture-specific libraries.

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Chapter 1

Functional Categories

This section categorizes, by function, the circuit design elements described in detail later in this guide. The elements (*primitives* and *macros*) are listed in alphanumeric order under each functional category.

Arithmetic

Design Element	Description
ACC1	Macro: 1-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset
ACC16	Macro: 16-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset
ACC4	Macro: 4-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset
ACC8	Macro: 8-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset
ADD1	Macro: 1-Bit Full Adder with Carry-In and Carry-Out
ADD16	Macro: 16-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow
ADD4	Macro: 4-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow
ADD8	Macro: 8-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow
ADSU1	Macro: 1-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out
ADSU16	Macro: 16-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out, and Overflow
ADSU4	Macro: 4-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out, and Overflow
ADSU8	Macro: 8-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out, and Overflow

Buffer

Design Element	Description
BUF	Primitive: General Purpose Buffer
BUF16	Macro: 16-Bit General Purpose Buffer
BUF4	Macro: 4-Bit General Purpose Buffer
BUF8	Macro: 8-Bit General Purpose Buffer
BUFE	Primitive: Internal 3-State Buffer with Active High Enable
BUFE16	Macro: 16-Bit Internal 3-State Buffer with Active High Enable
BUFE4	Macro: 4-BitInternal 3-State Buffer with Active High Enable
BUFE8	Macro: 8-Bit Internal 3-State Buffer with Active High Enable
BUFG	Primitive: Global Clock Buffer
BUFGSR	Primitive: Global Set/Reset Input Buffer
BUFGTS	Primitive: Global 3-State Input Buffer
BUFT	Primitive: Internal 3-State Buffer with Active Low Enable
BUFT16	Macro: 16-Bit Internal 3-State Buffers with Active Low Enable
BUFT4	Macro: 4-Bit Internal 3-State Buffers with Active Low Enable
BUFT8	Macro: 8-Bit Internal 3-State Buffers with Active Low Enable

Clock Divider

Design Element	Description
CLK_DIV10	Primitive: Simple Global Clock Divide by 10
CLK_DIV10R	Primitive: Global Clock Divide by 10 with Synchronous Reset
CLK_DIV10RSD	Primitive: Global Clock Divide by 10 with Synchronous Reset and Start Delay
CLK_DIV10SD	Primitive: Global Clock Divide by 10 with Start Delay
CLK_DIV12	Primitive: Simple Global Clock Divide by 12
CLK_DIV12R	Primitive: Global Clock Divide by 12 with Synchronous Reset
CLK_DIV12RSD	Primitive: Global Clock Divide by 12 with Synchronous Reset and Start Delay
CLK_DIV12SD	Primitive: Global Clock Divide by 12 with Start Delay
CLK_DIV14	Primitive: Simple Global Clock Divide by 14
CLK_DIV14R	Primitive: Global Clock Divide by 14 with Synchronous Reset
CLK_DIV14RSD	Primitive: Global Clock Divide by 14 with Synchronous Reset and Start Delay
CLK_DIV14SD	Primitive: Global Clock Divide by 14 with Start Delay

Design Element	Description
CLK_DIV16	Primitive: Simple Global Clock Divide by 16
CLK_DIV16R	Primitive: Global Clock Divide by 16 with Synchronous Reset
CLK_DIV16RSD	Primitive: Global Clock Divide by 16 with Synchronous Reset and Start Delay
CLK_DIV16SD	Primitive: Global Clock Divide by 16 with Start Delay
CLK_DIV2	Primitive: Simple Global Clock Divide by 2
CLK_DIV2R	Primitive: Global Clock Divide by 2 with Synchronous Reset
CLK_DIV2RSD	Primitive: Global Clock Divide by 2 with Synchronous Reset and Start Delay
CLK_DIV2SD	Primitive: Global Clock Divide by 2 with Start Delay
CLK_DIV4	Primitive: Simple Global Clock Divide by 4
CLK_DIV4R	Primitive: Global Clock Divide by 4 with Synchronous Reset
CLK_DIV4RSD	Primitive: Global Clock Divide by 4 with Synchronous Reset and Start Delay
CLK_DIV4SD	Primitive: Global Clock Divide by 4 with Start Delay
CLK_DIV6	Primitive: Simple Global Clock Divide by 6
CLK_DIV6R	Primitive: Global Clock Divide by 6 with Synchronous Reset
CLK_DIV6RSD	Primitive: Global Clock Divide by 6 with Synchronous Reset and Start Delay
CLK_DIV6SD	Primitive: Global Clock Divide by 6 with Start Delay
CLK_DIV8	Primitive: Simple Global Clock Divide by 8
CLK_DIV8R	Primitive: Global Clock Divide by 8 with Synchronous Reset
CLK_DIV8RSD	Primitive: Global Clock Divide by 8 with Synchronous Reset and Start Delay
CLK_DIV8SD	Primitive: Global Clock Divide by 8 with Start Delay

Comparator

Design Element	Description
COMP16	Macro: 16-Bit Identity Comparator
COMP2	Macro: 2-Bit Identity Comparator
COMP4	Macro: 4-Bit Identity Comparator
COMP8	Macro: 8-Bit Identity Comparator
COMPM16	Macro: 16-Bit Magnitude Comparator
COMPM2	Macro: 2-Bit Magnitude Comparator
COMPM4	Macro: 4-Bit Magnitude Comparator
COMPM8	Macro: 8-Bit Magnitude Comparator

Counter

Design Element	Description
CB16CE	Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CB16CLE	Macro: 16-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear
CB16CLED	Macro: 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear
CB16RE	Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset
CB16RLE	Macro: 16-Bit Loadable Cascadable Binary Counter with Clock Enable and Synchronous Reset
CB16X1	Macro: 16-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear
CB16X2	Macro: 16-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Synchro-nous Reset
CB2CE	Macro: 2-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CB2CLE	Macro: 2-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear
CB2CLED	Macro: 2-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear
CB2RE	Macro: 2-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset
CB2RLE	Macro: 2-Bit Loadable Cascadable Binary Counter with Clock Enable and Synchronous Reset
CB2X1	Macro: 2-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear
CB2X2	Macro: 2-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Synchronous Reset
CB4CE	Macro: 4-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CB4CLE	Macro: 4-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear
CB4CLED	Macro: 4-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear
CB4RE	Macro: 4-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset
CB4RLE	Macro: 4-Bit Loadable Cascadable Binary Counter with Clock Enable and Synchronous Reset
CB4X1	Macro: 4-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear
CB4X2	Macro: 4-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Synchronous Reset
CB8CE	Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CB8CLE	Macro: 8-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear

Design Element	Description
CB8CLED	Macro: 8-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear
CB8RE	Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset
CB8RLE	Macro: 8-Bit Loadable Cascadable Binary Counter with Clock Enable and Synchronous Reset
CB8X1	Macro: 8-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear
CB8X2	Macro: 8-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Synchronous Reset
CBD16CE	Macro: 16-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear
CBD16CLE	Macro: 16-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear
CBD16CLED	Macro: 16-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear
CBD16RE	Macro: 16-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset
CBD16RLE	Macro: 16-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset
CBD16X1	Macro: 16-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear
CBD16X2	Macro: 16-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset
CBD2CE	Macro: 2-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear
CBD2CLE	Macro: 2-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear
CBD2CLED	Macro: 2-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear
CBD2RE	Macro: 2-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset
CBD2RLE	Macro: 2-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset
CBD2X1	Macro: 2-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear
CBD2X2	Macro: 2-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset
CBD4CE	Macro: 4-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear
CBD4CLE	Macro: 4-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear

Design Element	Description
CBD4CLED	Macro: 4-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear
CBD4RE	Macro: 4-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset
CBD4RLE	Macro: 4-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset
CBD4X1	Macro: 4-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear
CBD4X2	Macro: 4-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset
CBD8CE	Macro: 8-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear
CBD8CLE	Macro: 8-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear
CBD8CLED	Macro: 8-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear
CBD8RE	Macro: 8-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset
CBD8RLE	Macro: 8-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset
CBD8X1	Macro: 8-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear
CBD8X2	Macro: 8-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset
CD4CE	Macro: 4-Bit Cascadable BCD Counter with Clock Enable and Asynchronous Clear
CD4CLE	Macro: 4-Bit Loadable Cascadable BCD Counter with Clock Enable and Asynchronous Clear
CD4RE	Macro: 4-Bit Cascadable BCD Counter with Clock Enable and Synchronous Reset
CD4RLE	Macro: 4-Bit Loadable Cascadable BCD Counter with Clock Enable and Synchronous Reset
CDD4CE	Macro: 4-Bit Cascadable Dual Edge Triggered BCD Counter with Clock Enable and Asynchronous Clear
CDD4CLE	Macro: 4-Bit Loadable Cascadable Dual Edge Triggered BCD Counter with Clock Enable and Asynchronous Clear
CDD4RE	Macro: 4-Bit Cascadable Dual Edge Triggered BCD Counter with Clock Enable and Synchronous Reset
CDD4RLE	Macro: 4-Bit Loadable Cascadable Dual Edge Triggered BCD Counter with Clock Enable and Synchronous Reset
CJ4CE	4-Bit Johnson Counter with Clock Enable and Asynchronous Clear

Design Element	Description
CJ4RE	Macro: 4-Bit Johnson Counter with Clock Enable and Synchronous Reset
CJ5CE	Macro: 5-Bit Johnson Counter with Clock Enable and Asynchronous Clear
CJ5RE	Macro: 5-Bit Johnson Counter with Clock Enable and Synchronous Reset
CJ8CE	Macro: 8-Bit Johnson Counter with Clock Enable and Asynchronous Clear
CJ8RE	Macro: 8-Bit Johnson Counter with Clock Enable and Synchronous Reset
CJD4CE	Macro: 4-Bit Dual Edge Triggered Johnson Counter with Clock Enable and Asynchronous Clear
CJD4RE	Macro: 4-Bit Dual Edge Triggered Johnson Counter with Clock Enable and Synchronous Reset
CJD5CE	Macro: 5-Bit Dual Edge Triggered Johnson Counter with Clock Enable and Asynchronous Clear
CJD5RE	Macro: 5-Bit Dual Edge Triggered Johnson Counter with Clock Enable and Synchronous Reset
CJD8CE	Macro: 8-Bit Dual Edge Triggered Johnson Counter with Clock Enable and Asynchronous Clear
CJD8RE	Macro: 8-Bit Dual Edge Triggered Johnson Counter with Clock Enable and Synchronous Reset
CR16CE	Macro: 16-Bit Negative-Edge Binary Ripple Counter with Clock Enable and Asynchronous Clear
CR8CE	Macro: 8-Bit Negative-Edge Binary Ripple Counter with Clock Enable and Asynchronous Clear
CRD16CE	Macro: 16-Bit Dual-Edge Triggered Binary Ripple Counter with Clock Enable and Asynchronous Clear
CRD8CE	Macro: 8-Bit Dual-Edge Triggered Binary Ripple Counter with Clock Enable and Asynchronous Clear

Decoder

Design Element	Description
D2_4E	Macro: 2- to 4-Line Decoder/Demultiplexer with Enable
D3_8E	Macro: 3- to 8-Line Decoder/Demultiplexer with Enable
D4_16E	Macro: 4- to 16-Line Decoder/Demultiplexer with Enable

Flip Flop

Design Element	Description
FD	Unknown type: D Flip-Flop
FD16	Macro: Multiple D Flip-Flop
FD16CE	Macro: 16-Bit Data Register with Clock Enable and Asynchronous Clear

Design Element	Description
FD16RE	Macro: 16-Bit Data Register with Clock Enable and Synchronous Reset
FD4	Macro: Multiple D Flip-Flop
FD4CE	Macro: 4-Bit Data Register with Clock Enable and Asynchronous Clear
FD4RE	Macro: 4-Bit Data Register with Clock Enable and Synchronous Reset
FD8	Macro: Multiple D Flip-Flop
FD8CE	Macro: 8-Bit Data Register with Clock Enable and Asynchronous Clear
FD8RE	Macro: 8-Bit Data Register with Clock Enable and Synchronous Reset
FDC	Unknown type: D Flip-Flop with Asynchronous Clear
FDCE	Primitive: D Flip-Flop with Clock Enable and Asynchronous Clear
FDCP	Primitive: D Flip-Flop with Asynchronous Preset and Clear
FDCPE	Primitive: D Flip-Flop with Clock Enable and Asynchronous Preset and Clear
FDD	Macro: Dual Edge Triggered D Flip-Flop
FDD16	Macro: Multiple Dual Edge Triggered D Flip-Flop
FDD16CE	Macro: 16-Bit Dual Edge Triggered Data Register with Clock Enable and Asynchronous Clear
FDD16RE	Macro: 16-Bit Dual Edge Triggered Data Register with Clock Enable and Synchronous Reset
FDD4	Multiple Dual Edge Triggered D Flip-Flop
FDD4CE	Macro: 4-Bit Dual Edge Triggered Data Register with Clock Enable and Asynchronous Clear
FDD4RE	Macro: 4-Bit Dual Edge Triggered Data Register with Clock Enable and Synchronous Reset
FDD8	Macro: Multiple Dual Edge Triggered D Flip-Flop
FDD8CE	Macro: 8-Bit Dual Edge Triggered Data Register with Clock Enable and Asynchronous Clear
FDD8RE	Macro: 8-Bit Dual Edge Triggered Data Register with Clock Enable and Synchronous Reset
FDDC	Macro: D Dual Edge Triggered Flip-Flop with Asynchronous Clear
FDDCE	Primitive: Dual Edge Triggered D Flip-Flop with Clock Enable and Asynchronous Clear
FDDCP	Primitive: Dual Edge Triggered D Flip-Flop Asynchronous Preset and Clear
FDDCPE	Macro: Dual Edge Triggered D Flip-Flop with Clock Enable and Asynchronous Preset and Clear
FDDP	Macro: Dual Edge Triggered D Flip-Flop with Asynchronous Preset
FDDPE	Primitive: Dual Edge Triggered D Flip-Flop with Clock Enable and Asynchronous Preset

Design Element	Description
FDDR	Macro: Dual Edge Triggered D Flip-Flop with Synchronous Reset
FDDRE	Macro: Dual Edge Triggered D Flip-Flop with Clock Enable and Synchronous Reset
FDDRS	Macro: Dual Edge Triggered D Flip-Flop with Synchronous Reset and Set
FDDRSE	Macro: Dual Edge Triggered D Flip-Flop with Synchronous Reset and Set and Clock Enable
FDDS	Macro: Dual Edge Triggered D Flip-Flop with Synchronous Set
FDDSE	Macro: D Flip-Flop with Clock Enable and Synchronous Set
FDDSR	Macro: Dual Edge Triggered D Flip-Flop with Synchronous Set and Reset
FDDSRE	Macro: Dual Edge Triggered D Flip-Flop with Synchronous Set and Reset and Clock Enable
FDP	Unknown type: D Flip-Flop with Asynchronous Preset
FDPE	Primitive: D Flip-Flop with Clock Enable and Asynchronous Preset
FDR	Unknown type: D Flip-Flop with Synchronous Reset
FDRE	Unknown type: D Flip-Flop with Clock Enable and Synchronous Reset
FDRS	Unknown type: Macro: D Flip-Flop with Synchronous Reset and Set
FDRSE	Unknown type: D Flip-Flop with Synchronous Reset and Set and Clock Enable
FDS	Unknown type: D Flip-Flop with Synchronous Set
FDSE	Unknown type: D Flip-Flop with Clock Enable and Synchronous Set
FDSR	D Flip-Flop with Synchronous Set and Reset
FDSRE	Macro: D Flip-Flop with Synchronous Set and Reset and Clock Enable
FJKC	Macro: J-K Flip-Flop with Asynchronous Clear
FJKCE	Macro: J-K Flip-Flop with Clock Enable and Asynchronous Clear
FJKCP	Macro: J-K Flip-Flop with Asynchronous Clear and Preset
FJKCPE	Macro: J-K Flip-Flop with Asynchronous Clear and Preset and Clock Enable
FJKP	Macro: J-K Flip-Flop with Asynchronous Preset
FJKPE	Macro: J-K Flip-Flop with Clock Enable and Asynchronous Preset
FJKRSE	Macro: J-K Flip-Flop with Clock Enable and Synchronous Reset and Set
FJKSRE	Macro: J-K Flip-Flop with Clock Enable and Synchronous Set and Reset
FTC	Macro: Toggle Flip-Flop with Asynchronous Clear

Design Element	Description
FTCE	Macro: Toggle Flip-Flop with Clock Enable and Asynchronous Clear
FTCLE	Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear
FTCLEX	Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear
FTCP	Primitive: Toggle Flip-Flop with Asynchronous Clear and Preset
FTCPE	Macro: Toggle Flip-Flop with Clock Enable and Asynchronous Clear and Preset
FTCPLE	Macro: Loadable Toggle Flip-Flop with Clock Enable and Asynchronous Clear and Preset
FTDCE	Macro: Dual-Edge Triggered Toggle Flip-Flop with Clock Enable and Asynchronous Clear
FTDCLE	Macro: Dual-Edge Triggered Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear
FTDCLEX	Macro: Dual-Edge Triggered Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear
FTDCP	Primitive: Dual-Edge Triggered Toggle Flip-Flop with Asynchronous Clear and Preset
FTDRSE	Macro: Dual-Edge Triggered Toggle Flip-Flop with Synchronous Reset, Set, and Clock Enable
FTDRSLE	Macro: Dual-Edge Triggered Toggle Flip-Flop with Clock Enable and Synchronous Reset and Set
FTP	Macro: Toggle Flip-Flop with Asynchronous Preset
FTPE	Macro: Toggle Flip-Flop with Clock Enable and Asynchronous Preset
FTPLE	Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Preset
FTRSE	Macro: Toggle Flip-Flop with Clock Enable and Synchronous Reset and Set
FTRSLE	Macro: Toggle/Loadable Flip-Flop with Clock Enable and Synchronous Reset and Set
FTSRE	Macro: Toggle Flip-Flop with Clock Enable and Synchronous Set and Reset
FTSRLE	Macro: Toggle/Loadable Flip-Flop with Clock Enable and Synchronous Set and Reset

General

Design Element	Description
GND	Primitive: Ground-Connection Signal Tag
KEEPER	Primitive: KEEPER Symbol
PULLDOWN	Primitive: Resistor to GND for Input Pads, Open-Drain, and 3-State Outputs
PULLUP	Primitive: Resistor to VCC for Input PADs, Open-Drain, and 3-State Outputs
VCC	Primitive: VCC-Connection Signal Tag

I/O

Design Element	Description
IBUF	Primitive: Input Buffer
IBUF16	Macro: 16-Bit Input Buffer
IBUF4	Macro: 4-Bit Input Buffer
IBUF8	Macro: 8-Bit Input Buffer
IOBUFE	Primitive: Bi-Directional Buffer
OBUF	Primitive: Output Buffer
OBUF16	Macro: 16-Bit Output Buffer
OBUF4	Macro: 4-Bit Output Buffer
OBUF8	Macro: 8-Bit Output Buffer
OBUFE	Macro: 3-State Output Buffer with Active-High Output Enable
OBUFE16	Macro: 16-Bit 3-State Output Buffer with Active-High Output Enable
OBUFE4	Macro: 4-Bit 3-State Output Buffer with Active-High Output Enable
OBUFE8	Macro: 8-Bit 3-State Output Buffer with Active-High Output Enable
OBUFT	Primitive: 3-State Output Buffer with Active Low Output Enable
OBUFT16	Macro: 16-Bit 3-State Output Buffer with Active Low Output Enable
OBUFT4	Macro: 4-Bit 3-State Output Buffers with Active-Low Output Enable
OBUFT8	Macro: 8-Bit 3-State Output Buffers with Active-Low Output Enable

Latch

Design Element	Description
LD	Primitive: Transparent Data Latch
LD16	Macro: Multiple Transparent Data Latch
LD4	Macro: Multiple Transparent Data Latch
LD8	Macro: Multiple Transparent Data Latch
LDC	Primitive: Macro: Transparent Data Latch with Asynchronous Clear
LDCP	Primitive: Transparent Data Latch with Asynchronous Clear and Preset
LDG	Primitive: Transparent Datagate Latch
LDG16	Macro: 16-bit Transparent Datagate Latch
LDG4	Macro: 4-Bit Transparent Datagate Latch
LDG8	Macro: 8-Bit Transparent Datagate Latch
LDP	Primitive: Macro: Transparent Data Latch with Asynchronous Preset

Logic

Design Element	Description
AND2	Primitive: 2-Input AND Gate with Non-Inverted Inputs
AND2B1	Primitive: 2-Input AND Gate with 1 Inverted and 1 Non-Inverted Inputs
AND2B2	Primitive: 2-Input AND Gate with Inverted Inputs
AND3	Primitive: 3-Input AND Gate with Non-Inverted Inputs
AND3B1	Primitive: 3-Input AND Gate with 1 Inverted and 2 Non-Inverted Inputs
AND3B2	Primitive: 3-Input AND Gate with 2 Inverted and 1 Non-Inverted Inputs
AND3B3	Primitive: 3-Input AND Gate with Inverted Inputs
AND4	Primitive: 4-Input AND Gate with Non-Inverted Inputs
AND4B1	Primitive: 4-Input AND Gate with 1 Inverted and 3 Non-Inverted Inputs
AND4B2	Primitive: 4-Input AND Gate with 2 Inverted and 2 Non-Inverted Inputs
AND4B3	Primitive: 4-Input AND Gate with 3 Inverted and 1 Non-Inverted Inputs
AND4B4	Primitive: 4-Input AND Gate with Inverted Inputs
AND5	Primitive: 5-Input AND Gate with Non-Inverted Inputs
AND5B1	Primitive: 5-Input AND Gate with 1 Inverted and 4 Non-Inverted Inputs
AND5B2	Primitive: 5-Input AND Gate with 2 Inverted and 3 Non-Inverted Inputs

Design Element	Description
AND5B3	Primitive: 5-Input AND Gate with 3 Inverted and 2 Non-Inverted Inputs
AND5B4	Primitive: 5-Input AND Gate with 4 Inverted and 1 Non-Inverted Inputs
AND5B5	Primitive: 5-Input AND Gate with Inverted Inputs
AND6	Macro: 6-Input AND Gate with Non-Inverted Inputs
AND7	Macro: 7-Input AND Gate with Non-Inverted Inputs
AND8	Macro: 8-Input AND Gate with Non-Inverted Inputs
AND9	Macro: 9-Input AND Gate with Non-Inverted Inputs
INV	Primitive: Inverter
INV16	Macro: 16 Inverters
INV4	Macro: Four Inverters
INV8	Macro: Eight Inverters
NAND2	Primitive: 2-Input NAND Gate with Non-Inverted Inputs
NAND2B1	Primitive: 2-Input NAND Gate with 1 Inverted and 1 Non-Inverted Inputs
NAND2B2	Primitive: 2-Input NAND Gate with Inverted Inputs
NAND3	Primitive: 3-Input NAND Gate with Non-Inverted Inputs
NAND3B1	Primitive: 3-Input NAND Gate with 1 Inverted and 2 Non-Inverted Inputs
NAND3B2	Primitive: 3-Input NAND Gate with 2 Inverted and 1 Non-Inverted Inputs
NAND3B3	Primitive: 3-Input NAND Gate with Inverted Inputs
NAND4	Primitive: 4-Input NAND Gate with Non-Inverted Inputs
NAND4B1	Primitive: 4-Input NAND Gate with 1 Inverted and 3 Non-Inverted Inputs
NAND4B2	Primitive: 4-Input NAND Gate with 2 Inverted and 2 Non-Inverted Inputs
NAND4B3	Primitive: 4-Input NAND Gate with 3 Inverted and 1 Non-Inverted Inputs
NAND4B4	Primitive: 4-Input NAND Gate with Inverted Inputs
NAND5	Primitive: 5-Input NAND Gate with Non-Inverted Inputs
NAND5B1	Primitive: 5-Input NAND Gate with 1 Inverted and 4 Non-Inverted Inputs
NAND5B2	Primitive: 5-Input NAND Gate with 2 Inverted and 3 Non-Inverted Inputs
NAND5B3	Primitive: 5-Input NAND Gate with 3 Inverted and 2 Non-Inverted Inputs
NAND5B4	Primitive: 5-Input NAND Gate with 4 Inverted and 1 Non-Inverted Inputs
NAND5B5	Primitive: 5-Input NAND Gate with Inverted Inputs
NAND6	Macro: 6-Input NAND Gate with Non-Inverted Inputs
NAND7	Macro: 7-Input NAND Gate with Non-Inverted Inputs

Design Element	Description
NAND8	Macro: 8-Input NAND Gate with Non-Inverted Inputs
NAND9	Macro: 9-Input NAND Gate with Non-Inverted Inputs
NOR2	Primitive: 2-Input NOR Gate with Non-Inverted Inputs
NOR2B1	Primitive: 2-Input NOR Gate with 1 Inverted and 1 Non-Inverted Inputs
NOR2B2	Primitive: 2-Input NOR Gate with Inverted Inputs
NOR3	Primitive: 3-Input NOR Gate with Non-Inverted Inputs
NOR3B1	Primitive: 3-Input NOR Gate with 1 Inverted and 2 Non-Inverted Inputs
NOR3B2	Primitive: 3-Input NOR Gate with 2 Inverted and 1 Non-Inverted Inputs
NOR3B3	Primitive: 3-Input NOR Gate with Inverted Inputs
NOR4	Primitive: 4-Input NOR Gate with Non-Inverted Inputs
NOR4B1	Primitive: 4-Input NOR Gate with 1 Inverted and 3 Non-Inverted Inputs
NOR4B2	Primitive: 4-Input NOR Gate with 2 Inverted and 2 Non-Inverted Inputs
NOR4B3	Primitive: 4-Input NOR Gate with 3 Inverted and 1 Non-Inverted Inputs
NOR4B4	Primitive: 4-Input NOR Gate with Inverted Inputs
NOR5	Primitive: 5-Input NOR Gate with Non-Inverted Inputs
NOR5B1	Primitive: 5-Input NOR Gate with 1 Inverted and 4 Non-Inverted Inputs
NOR5B2	Primitive: 5-Input NOR Gate with 2 Inverted and 3 Non-Inverted Inputs
NOR5B3	Primitive: 5-Input NOR Gate with 3 Inverted and 2 Non-Inverted Inputs
NOR5B4	Primitive: 5-Input NOR Gate with 4 Inverted and 1 Non-Inverted Inputs
NOR5B5	Primitive: 5-Input NOR Gate with Inverted Inputs
NOR6	Macro: 6-Input NOR Gate with Non-Inverted Inputs
NOR7	Macro: 7-Input NOR Gate with Non-Inverted Inputs
NOR8	Macro: 8-Input NOR Gate with Non-Inverted Inputs
NOR9	Macro: 9-Input NOR Gate with Non-Inverted Inputs
OR2	Primitive: 2-Input OR Gate with Non-Inverted Inputs
OR2B1	Primitive: 2-Input OR Gate with 1 Inverted and 1 Non-Inverted Inputs
OR2B2	Primitive: 2-Input OR Gate with Inverted Inputs
OR3	Primitive: 3-Input OR Gate with Non-Inverted Inputs
OR3B1	Primitive: 3-Input OR Gate with 1 Inverted and 2 Non-Inverted Inputs
OR3B2	Primitive: 3-Input OR Gate with 2 Inverted and 1 Non-Inverted Inputs

Design Element	Description
OR3B3	Primitive: 3-Input OR Gate with Inverted Inputs
OR4	Primitive: 4-Input OR Gate with Non-Inverted Inputs
OR4B1	Primitive: 4-Input OR Gate with 1 Inverted and 3 Non-Inverted Inputs
OR4B2	Primitive: 4-Input OR Gate with 2 Inverted and 2 Non-Inverted Inputs
OR4B3	Primitive: 4-Input OR Gate with 3 Inverted and 1 Non-Inverted Inputs
OR4B4	Primitive: 4-Input OR Gate with Inverted Inputs
OR5	Primitive: 5-Input OR Gate with Non-Inverted Inputs
OR5B1	Primitive: 5-Input OR Gate with 1 Inverted and 4 Non-Inverted Inputs
OR5B2	Primitive: 5-Input OR Gate with 2 Inverted and 3 Non-Inverted Inputs
OR5B3	Primitive: 5-Input OR Gate with 3 Inverted and 2 Non-Inverted Inputs
OR5B4	Primitive: 5-Input OR Gate with 4 Inverted and 1 Non-Inverted Inputs
OR5B5	Primitive: 5-Input OR Gate with Inverted Inputs
OR6	Macro: 6-Input OR Gate with Non-Inverted Inputs
OR7	Macro: 7-Input OR Gate with Non-Inverted Inputs
OR8	Macro: 8-Input OR Gate with Non-Inverted Inputs
OR9	Macro: 9-Input OR Gate with Non-Inverted Inputs
XNOR2	Primitive: 2-Input XNOR Gate with Non-Inverted Inputs
XNOR3	Primitive: 3-Input XNOR Gate with Non-Inverted Inputs
XNOR4	Primitive: 4-Input XNOR Gate with Non-Inverted Inputs
XNOR5	Primitive: 5-Input XNOR Gate with Non-Inverted Inputs
XNOR6	Macro: 6-Input XNOR Gate with Non-Inverted Inputs
XNOR7	Macro: 7-Input XNOR Gate with Non-Inverted Inputs
XNOR8	Macro: 8-Input XNOR Gate with Non-Inverted Inputs
XNOR9	Macro: 9-Input XNOR Gate with Non-Inverted Inputs
XOR2	Primitive: 2-Input XOR Gate with Non-Inverted Inputs
XOR3	Primitive: 3-Input XOR Gate with Non-Inverted Inputs
XOR4	Primitive: 4-Input XOR Gate with Non-Inverted Inputs
XOR5	Primitive: 5-Input XOR Gate with Non-Inverted Inputs
XOR6	Macro: 6-Input XOR Gate with Non-Inverted Inputs
XOR7	Macro: 7-Input XOR Gate with Non-Inverted Inputs
XOR8	Macro: 8-Input XOR Gate with Non-Inverted Inputs
XOR9	Macro: 9-Input XOR Gate with Non-Inverted Inputs

Mux

Design Element	Description
M16_1E	Macro: 16-to-1 Multiplexer with Enable
M2_1	Macro: 2-to-1 Multiplexer
M2_1B1	Macro: 2-to-1 Multiplexer with D0 Inverted
M2_1B2	Macro: 2-to-1 Multiplexer with D0 and D1 Inverted
M2_1E	Macro: 2-to-1 Multiplexer with Enable
M4_1E	Macro: 4-to-1 Multiplexer with Enable
M8_1E	Macro: 8-to-1 Multiplexer with Enable

Shift Register

Design Element	Description
SR16CE	Macro: 16-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR16CLE	Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR16CLED	Macro: 16-Bit Shift Register with Clock Enable and Asynchronous Clear
SR16RE	Macro: 16-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR16RLE	Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR16RLED	Macro: 16-Bit Shift Register with Clock Enable and Synchronous Reset
SR4CE	Macro: 4-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR4CLE	Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR4CLED	Macro: 4-Bit Shift Register with Clock Enable and Asynchronous Clear
SR4RE	Macro: 4-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR4RLE	Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR4RLED	Macro: 4-Bit Shift Register with Clock Enable and Synchronous Reset
SR8CE	Macro: 8-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR8CLE	Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR8CLED	Macro: 8-Bit Shift Register with Clock Enable and Asynchronous Clear
SR8RE	Macro: 8-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset

Design Element	Description
SR8RLE	Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR8RLED	Macro: 8-Bit Shift Register with Clock Enable and Synchronous Reset
SRD16CE	Macro: 16-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear
SRD16CLE	Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear
SRD16CLED	Macro: 16-Bit Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear
SRD16RE	Macro: 16-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset
SRD16RLE	Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset
SRD16RLED	Macro: 16-Bit Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset
SRD4CE	Macro: 4-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear
SRD4CLE	Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear
SRD4CLED	Macro: 4-Bit Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear
SRD4RE	Macro: 4-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset
SRD4RLE	Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset
SRD4RLED	Macro: 4-Bit Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset
SRD8CE	Macro: 8-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear
SRD8CLE	Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear
SRD8CLED	Macro: 8-Bit Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear
SRD8RE	Macro: 8-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset
SRD8RLE	Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset
SRD8RLED	Macro: 8-Bit Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset

Shifter

Design Element	Description
BRLSHFT4	Macro: 4-Bit Barrel Shifter
BRLSHFT8	Macro: 8-Bit Barrel Shifter

About Design Elements

This section describes the design elements that can be used with this architecture. The design elements are organized alphabetically.

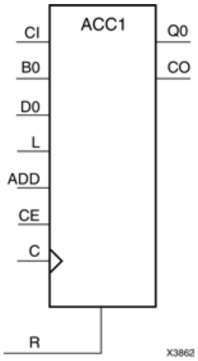
The following information is provided for each design element, where applicable:

- Name of element
- Brief description
- Schematic symbol (if any)
- Logic Table (if any)
- Port Descriptions (if any)
- Design Entry Method
- Available Attributes (if any)
- For more information

You can find examples of VHDL and Verilog instantiation code in the ISE software (in the main menu, select **Edit > Language Templates** or in the *Libraries Guide for HDL Designs* for this architecture.

ACC1

Macro: 1-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element can add or subtract a 1-bit unsigned-binary word to or from the contents of a 1-bit data register and store the results in the register. The register can be loaded with a 1-bit word. The synchronous reset (R) has priority over all other inputs and, when High, causes the output to go to logic level zero during the Low-to-High clock (C) transition. Clock (C) transitions are ignored when clock enable (CE) is Low.

Load

When the load input (L) is High, CE is ignored and the data on the input D0 is loaded into the 1-bit register during the Low-to-High clock (C) transition.

Add

When control inputs ADD and CE are both High, the accumulator adds a 1-bit word (B0) and carry-in (CI) to the contents of the 1-bit register. The result is stored in the register and appears on output Q0 during the Low-to-High clock transition. The carry-out (CO) is not registered synchronously with the data output. CO always reflects the accumulation of input B0 and the contents of the register, which allows cascading of ACC1s by connecting CO of one stage to CI of the next stage. In add mode, CO acts as a carry-out, and CO and CI are active-High.

Subtract

When ADD is Low and CE is High, the 1-bit word B0 and CI are subtracted from the contents of the register. The result is stored in the register and appears on output Q0 during the Low-to-High clock transition. The carry-out (CO) is not registered synchronously with the data output. CO always reflects the accumulation of input B0 and the contents of the register, which allows cascading of ACC1s by connecting CO of one stage to CI of the next stage. In subtract mode, CO acts as a borrow, and CO and CI are active-Low.

This design element is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Design Entry Method

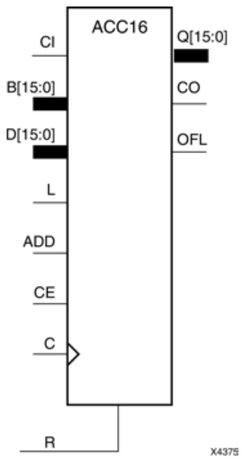
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

ACC16

Macro: 16-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element can add or subtract a 16-bit unsigned-binary, respectively or two's-complement word to or from the contents of a 16-bit data register and store the results in the register. The register can be loaded with the 16-bit word.

When the load input (L) is High, CE is ignored and the data on the D inputs is loaded into the register during the Low-to-High clock (C) transition. ACC16 loads the data on inputs D15 : D0 into the 16-bit register.

This design element operates on either 16-bit unsigned binary numbers or 16-bit two's-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is how they determine when "overflow" occurs. Unsigned binary uses carry-out (CO), while two's complement uses OFL to determine when "overflow" occurs.

- For unsigned binary operation, ACC16 can represent numbers between 0 and 15, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtracter. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds. The carry-out (CO) is not registered synchronously with the data outputs. CO always reflects the accumulation of the B inputs (B15 : B0 for ACC16). This allows the cascading of ACC16s by connecting CO of one stage to CI of the next stage. An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows:

  ```
  unsigned overflow = CO XOR ADD
  ```

  Ignore OFL in unsigned binary operation.

- For two's-complement operation, ACC16 represents numbers between -8 and +7, inclusive. If an addition or subtraction operation result exceeds this range, the OFL output goes High. The overflow (OFL) is not registered synchronously with the data outputs. OFL always reflects the accumulation of the B inputs (B15 : B0 for ACC16) and the contents of the register, which allows cascading of ACC4s by connecting OFL of one stage to CI of the next stage.

Ignore CO in two's-complement operation.

The synchronous reset (R) has priority over all other inputs, and when set to High, causes all outputs to go to logic level zero during the Low-to-High clock (C) transition. Clock (C) transitions are ignored when clock enable (CE) is Low.

This design element is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Input						Output
R	**L**	**CE**	**ADD**	**D**	**C**	**Q**
1	x	x	x	x	↑	0
0	1	x	x	Dn	↑	Dn
0	0	1	1	x	↑	Q0+Bn+CI
0	0	1	0	x	↑	Q0-Bn-CI
0	0	0	x	x	↑	No Change
Q0: Previous value of Q Bn: Value of Data input B CI: Value of input CI						

Design Entry Method

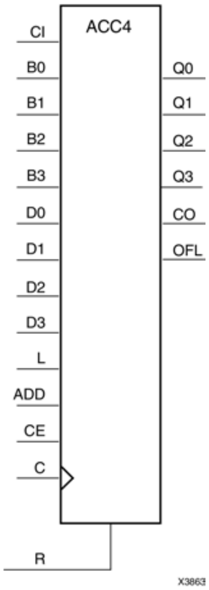
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

ACC4

Macro: 4-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element can add or subtract a 4-bit unsigned-binary, respectively or two's-complement word to or from the contents of a 4-bit data register and store the results in the register. The register can be loaded with the 4-bit word.

When the load input (L) is High, CE is ignored and the data on the D inputs is loaded into the register during the Low-to-High clock (C) transition. ACC4 loads the data on inputs D3 : D0 into the 4-bit register.

This design element operates on either 4-bit unsigned binary numbers or 4-bit two's-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is how they determine when "overflow" occurs. Unsigned binary uses carry-out (CO), while two's complement uses OFL to determine when "overflow" occurs.

- For unsigned binary operation, ACC4 can represent numbers between 0 and 15, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtracter. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds. The carry-out (CO) is not registered synchronously with the data outputs. CO always reflects the accumulation of the B inputs (B3 : B0 for ACC4). This allows the cascading of ACC4s by connecting CO of one stage to CI of the next stage. An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows:

  ```
  unsigned overflow = CO XOR ADD
  ```

  Ignore OFL in unsigned binary operation.

- For two's-complement operation, ACC4 represents numbers between -8 and +7, inclusive. If an addition or subtraction operation result exceeds this range, the OFL output goes High. The overflow (OFL) is not registered synchronously with the data outputs. OFL always reflects the accumulation of the B inputs (B3 : B0 for ACC4) and the contents of the register, which allows cascading of ACC4s by connecting OFL of one stage to CI of the next stage.

  Ignore CO in two's-complement operation.

The synchronous reset (R) has priority over all other inputs, and when set to High, causes all outputs to go to logic level zero during the Low-to-High clock (C) transition. Clock (C) transitions are ignored when clock enable (CE) is Low.

This design element is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Input						Output
R	**L**	**CE**	**ADD**	**D**	**C**	**Q**
1	x	x	x	x	↑	0
0	1	x	x	Dn	↑	Dn
0	0	1	1	x	↑	Q0+Bn+CI
0	0	1	0	x	↑	Q0-Bn-CI
0	0	0	x	x	↑	No Change
Q0: Previous value of Q Bn: Value of Data input B CI: Value of input CI						

Design Entry Method

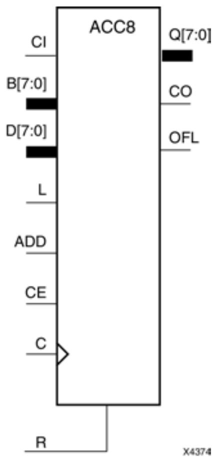
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

ACC8

Macro: 8-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element can add or subtract a 8-bit unsigned-binary, respectively or two's-complement word to or from the contents of a 8-bit data register and store the results in the register. The register can be loaded with the 8-bit word.

When the load input (L) is High, CE is ignored and the data on the D inputs is loaded into the register during the Low-to-High clock (C) transition. ACC8 loads the data on inputs D7 : D0 into the 8-bit register.

This design element operates on either 8-bit unsigned binary numbers or 8-bit two's-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is how they determine when "overflow" occurs. Unsigned binary uses carry-out (CO), while two's complement uses OFL to determine when "overflow" occurs.

- For unsigned binary operation, ACC8 can represent numbers between 0 and 255, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtracter. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds. The carry-out (CO) is not registered synchronously with the data outputs. CO always reflects the accumulation of the B inputs (B3 : B0 for ACC4). This allows the cascading of ACC8s by connecting CO of one stage to CI of the next stage. An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows:

  ```
  unsigned overflow = CO XOR ADD
  ```

  Ignore OFL in unsigned binary operation.

- For two's-complement operation, ACC8 represents numbers between -128 and +127, inclusive. If an addition or subtraction operation result exceeds this range, the OFL output goes High. The overflow (OFL) is not registered synchronously with the data outputs. OFL always reflects the accumulation of the B inputs (B3 : B0 for ACC8) and the contents of the register, which allows cascading of ACC8s by connecting OFL of one stage to CI of the next stage.

Ignore CO in two's-complement operation.

The synchronous reset (R) has priority over all other inputs, and when set to High, causes all outputs to go to logic level zero during the Low-to-High clock (C) transition. Clock (C) transitions are ignored when clock enable (CE) is Low.

This design element is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Input						Output
R	**L**	**CE**	**ADD**	**D**	**C**	**Q**
1	x	x	x	x	↑	0
0	1	x	x	Dn	↑	Dn
0	0	1	1	x	↑	Q0+Bn+CI
0	0	1	0	x	↑	Q0-Bn-CI
0	0	0	x	x	↑	No Change
Q0: Previous value of Q Bn: Value of Data input B CI: Value of input CI						

Design Entry Method

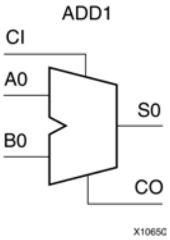
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

ADD1

Macro: 1-Bit Full Adder with Carry-In and Carry-Out



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a cascadable 1-bit full adder with carry-in and carry-out. It adds two 1-bit words (A and B) and a carry-in (CI), producing a binary sum (S0) output and a carry-out (CO).

Logic Table

Inputs			Outputs	
A0	**B0**	**CI**	**S0**	**CO**
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

Design Entry Method

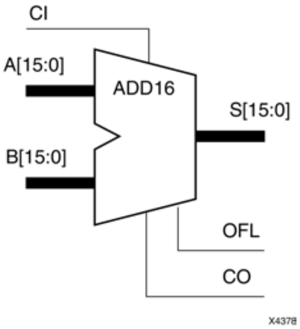
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

ADD16

Macro: 16-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element adds two words and a carry-in (CI), producing a sum output and carry-out (CO) or overflow (OFL). The factors added are A15:A0, B15:B0 and CI, producing the sum output S15:S0 and CO (or OFL).

Logic Table

Input		Output
A	**B**	**S**
An	Bn	An+Bn+CI
CI: Value of input CI.		

Unsigned Binary Versus Two's Complement -This design element can operate on either 16-bit unsigned binary numbers or 16-bit two's-complement numbers, respectively. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is the way they determine when "overflow" occurs. Unsigned binary uses CO, while two's-complement uses OFL to determine when "overflow" occurs. To interpret the inputs as unsigned binary, follow the CO output. To interpret the inputs as two's complement, follow the OFL output.

Unsigned Binary Operation -For unsigned binary operation, this element represents numbers between 0 and 65535, inclusive. OFL is ignored in unsigned binary operation.

Two's-Complement Operation -For two's-complement operation, this element can represent numbers between -32768 and +32767, inclusive. OFL is active (High) when the sum exceeds the bounds of the adder. CO is ignored in two's-complement operation.

Design Entry Method

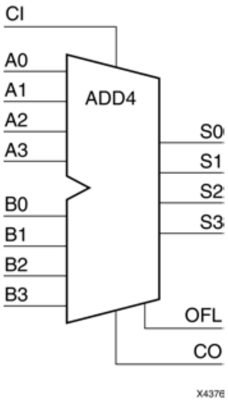
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

ADD4

Macro: 4-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element adds two words and a carry-in (CI), producing a sum output and carry-out (CO) or overflow (OFL). The factors added are A3:A0, B3:B0, and CI producing the sum output S3:S0 and CO (or OFL).

Logic Table

Input		Output
A	B	S
An	Bn	An+Bn+CI
CI: Value of input CI.		

Unsigned Binary Versus Two's Complement -This design element can operate on either 4-bit unsigned binary numbers or 4-bit two's-complement numbers, respectively. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is the way they determine when "overflow" occurs. Unsigned binary uses CO, while two's-complement uses OFL to determine when "overflow" occurs. To interpret the inputs as unsigned binary, follow the CO output. To interpret the inputs as two's complement, follow the OFL output.

Unsigned Binary Operation -For unsigned binary operation, this element represents numbers from 0 to 15, inclusive. OFL is ignored in unsigned binary operation.

Two's-Complement Operation -For two's-complement operation, this element can represent numbers between -8 and +7, inclusive. OFL is active (High) when the sum exceeds the bounds of the adder. CO is ignored in two's-complement operation.

Design Entry Method

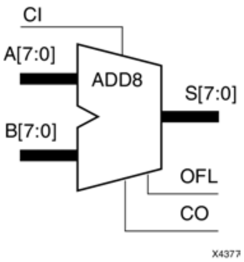
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

ADD8

Macro: 8-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element adds two words and a carry-in (CI), producing a sum output and carry-out (CO) or overflow (OFL). The factors added are A7:A0, B7:B0, and CI, producing the sum output S7:S0 and CO (or OFL).

Logic Table

Input		Output
A	**B**	**S**
An	Bn	An+Bn+CI
CI: Value of input CI.		

Unsigned Binary Versus Two's Complement -This design element can operate on either 8-bit unsigned binary numbers or 8-bit two's-complement numbers, respectively. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is the way they determine when "overflow" occurs. Unsigned binary uses CO, while two's-complement uses OFL to determine when "overflow" occurs. To interpret the inputs as unsigned binary, follow the CO output. To interpret the inputs as two's complement, follow the OFL output.

Unsigned Binary Operation -For unsigned binary operation, this element represents numbers between 0 and 255, inclusive. OFL is ignored in unsigned binary operation.

Two's-Complement Operation -For two's-complement operation, this element can represent numbers between -128 and +127, inclusive. OFL is active (High) when the sum exceeds the bounds of the adder. CO is ignored in two's-complement operation.

Design Entry Method

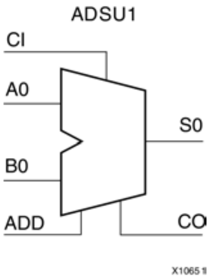
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

ADSU1

Macro: 1-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

When the ADD input is High, this element adds two 1-bit words (A0 and B0) with a carry-in (CI), producing a 1-bit output (S0) and a carry-out (CO). When the ADD input is Low, B0 is subtracted from A0, producing a result (S0) and borrow (CO).

In add mode, CO represents a carry-out, and CO and CI are active-High. In subtract mode, CO represents a borrow, and CO and CI are active-Low.

Add Function, ADD=1

Inputs			Outputs	
A0	**B0**	**CI**	**S0**	**CO**
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

Subtract Function, ADD=0

Inputs			Outputs	
A0	**B0**	**CI**	**S0**	**CO**
0	0	0	1	0
0	1	0	0	0
1	0	0	0	1
1	1	0	1	0
0	0	1	0	1
0	1	1	1	0
1	0	1	1	1
1	1	1	0	1
1	0	1	1	1
1	1	1	0	1

Design Entry Method

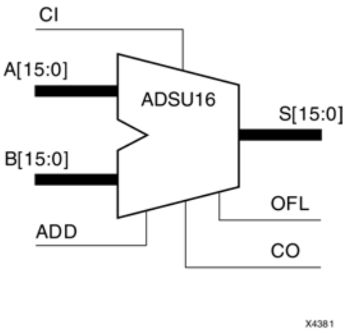
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

ADSU16

Macro: 16-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out, and Overflow



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

When the ADD input is High, this element adds two 16-bit words (A15:A0 and B15:B0) and a carry-in (CI), producing a 16-bit sum output (S15:S0) and carry-out (CO) or overflow (OFL).

When the ADD input is Low, this element subtracts B15:B0 from A15:A0, producing a difference output and a carry-out (CO) or an overflow (OFL).

In add mode, CO and CI are active-High. In subtract mode, CO and CI are active-Low. OFL is active-High in add and subtract modes.

Logic Table

Input			Output
ADD	**A**	**B**	**S**
1	An	Bn	An+Bn+CI*
0	An	Bn	An-Bn-CI*
CI*: ADD = 0, CI, CO active LOW			
CI*: ADD = 1, CI, CO active HIGH			

Unsigned Binary Versus Two's Complement -This design element can operate on either 16-bit unsigned binary numbers or 16-bit two's-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is the way they determine when "overflow" occurs. Unsigned binary uses CO, while two's complement uses OFL to determine when "overflow" occurs.

With adder/subtracters, either unsigned binary or two's-complement operations cause an overflow. If the result crosses the overflow boundary, an overflow is generated. Similarly, when the result crosses the carry-out boundary, a carry-out is generated.

Unsigned Binary Operation -For unsigned binary operation, this element can represent numbers between 0 and 65535, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtracter. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds.

An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows:

```
unsigned overflow = CO XOR ADD
```

OFL is ignored in unsigned binary operation.

Two's-Complement Operation -For two's-complement operation, this element can represent numbers between -32768 and +32767, inclusive.

If an addition or subtraction operation result exceeds this range, the OFL output goes High. CO is ignored in two's-complement operation.

Design Entry Method

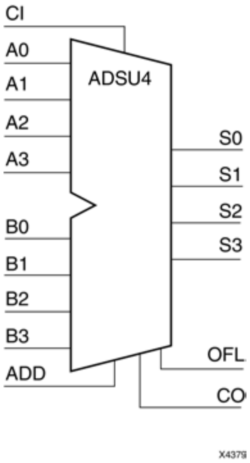
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

ADSU4

Macro: 4-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out, and Overflow



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

When the ADD input is High, this element adds two 4-bit words (A3:A0 and B3:B0) and a carry-in (CI), producing a 4-bit sum output (S3:S0) and a carry-out (CO) or an overflow (OFL).

When the ADD input is Low, this element subtracts B3:B0 from A3:A0, producing a 4-bit difference output (S3:S0) and a carry-out (CO) or an overflow (OFL).

In add mode, CO and CI are active-High. In subtract mode, CO and CI are active-Low. OFL is active-High in add and subtract modes.

Logic Table

Input			Output
ADD	**A**	**B**	**S**
1	An	Bn	An+Bn+CI*
0	An	Bn	An-Bn-CI*
CI*: ADD = 0, CI, CO active LOW			
CI*: ADD = 1, CI, CO active HIGH			

Unsigned Binary Versus Two's Complement -This design element can operate on either 4-bit unsigned binary numbers or 4-bit two's-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is the way they determine when "overflow" occurs. Unsigned binary uses CO, while two's complement uses OFL to determine when "overflow" occurs.

With adder/subtracters, either unsigned binary or two's-complement operations cause an overflow. If the result crosses the overflow boundary, an overflow is generated. Similarly, when the result crosses the carry-out boundary, a carry-out is generated.

Unsigned Binary Operation -For unsigned binary operation, ADSU4 can represent numbers between 0 and 15, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtracter. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds.

An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows:

```
unsigned overflow = CO XOR ADD
```

OFL is ignored in unsigned binary operation.

Two's-Complement Operation -For two's-complement operation, this element can represent numbers between -8 and +7, inclusive.

If an addition or subtraction operation result exceeds this range, the OFL output goes High. CO is ignored in two's-complement operation.

Design Entry Method

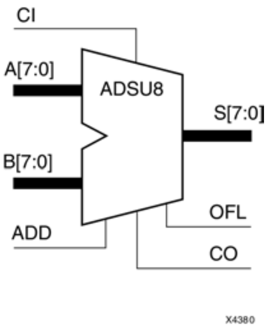
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

ADSU8

Macro: 8-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out, and Overflow



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

When the ADD input is High, this element adds two 8-bit words (A7:A0 and B7:B0) and a carry-in (CI), producing, an 8-bit sum output (S7:S0) and carry-out (CO) or an overflow (OFL).

When the ADD input is Low, this element subtracts B7:B0 from A7:A0, producing an 8-bit difference output (S7:S0) and a carry-out (CO) or an overflow (OFL).

In add mode, CO and CI are active-High. In subtract mode, CO and CI are active-Low. OFL is active-High in add and subtract modes.

Logic Table

Input			Output
ADD	**A**	**B**	**S**
1	An	Bn	An+Bn+CI*
0	An	Bn	An-Bn-CI*
CI*: ADD = 0, CI, CO active LOW			
CI*: ADD = 1, CI, CO active HIGH			

Unsigned Binary Versus Two's Complement -This design element can operate on either 8-bit unsigned binary numbers or 8-bit two's-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is the way they determine when "overflow" occurs. Unsigned binary uses CO, while two's complement uses OFL to determine when "overflow" occurs.

With adder/subtracters, either unsigned binary or two's-complement operations cause an overflow. If the result crosses the overflow boundary, an overflow is generated. Similarly, when the result crosses the carry-out boundary, a carry-out is generated.

Unsigned Binary Operation -For unsigned binary operation, this element can represent numbers between 0 and 255, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtracter. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds.

An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows:

```
unsigned overflow = CO XOR ADD
```

OFL is ignored in unsigned binary operation.

Two's-Complement Operation -For two's-complement operation, this element can represent numbers between -128 and +127, inclusive.

If an addition or subtraction operation result exceeds this range, the OFL output goes High. CO is ignored in two's-complement operation.

Design Entry Method

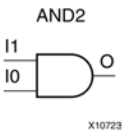
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

AND2

Primitive: 2-Input AND Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

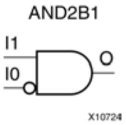
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

AND2B1

Primitive: 2-Input AND Gate with 1 Inverted and 1 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

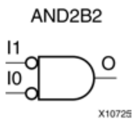
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

AND2B2

Primitive: 2-Input AND Gate with Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

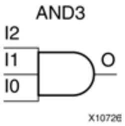
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

AND3

Primitive: 3-Input AND Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

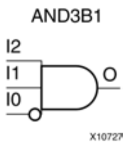
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

AND3B1

Primitive: 3-Input AND Gate with 1 Inverted and 2 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

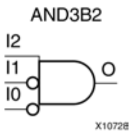
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

AND3B2

Primitive: 3-Input AND Gate with 2 Inverted and 1 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

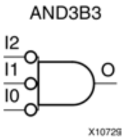
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

AND3B3

Primitive: 3-Input AND Gate with Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

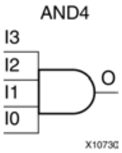
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

AND4

Primitive: 4-Input AND Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

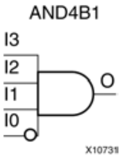
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

AND4B1

Primitive: 4-Input AND Gate with 1 Inverted and 3 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

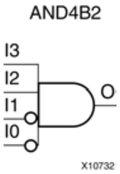
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

AND4B2

Primitive: 4-Input AND Gate with 2 Inverted and 2 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

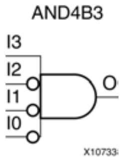
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

AND4B3

Primitive: 4-Input AND Gate with 3 Inverted and 1 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

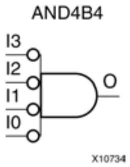
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

AND4B4

Primitive: 4-Input AND Gate with Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

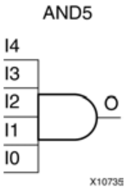
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

AND5

Primitive: 5-Input AND Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

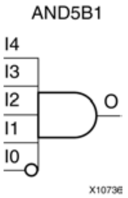
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

AND5B1

Primitive: 5-Input AND Gate with 1 Inverted and 4 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

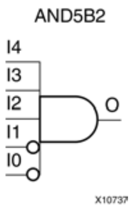
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

AND5B2

Primitive: 5-Input AND Gate with 2 Inverted and 3 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

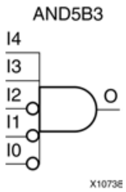
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

AND5B3

Primitive: 5-Input AND Gate with 3 Inverted and 2 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

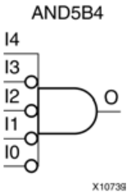
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

AND5B4

Primitive: 5-Input AND Gate with 4 Inverted and 1 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

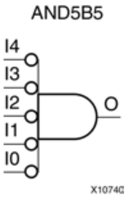
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

AND5B5

Primitive: 5-Input AND Gate with Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

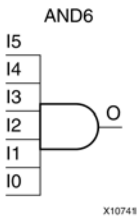
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

AND6

Macro: 6-Input AND Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

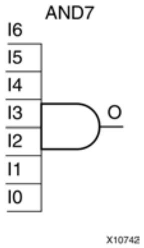
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

AND7

Macro: 7-Input AND Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

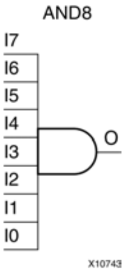
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

AND8

Macro: 8-Input AND Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

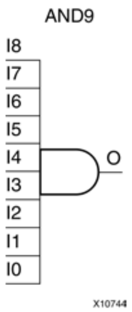
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

AND9

Macro: 9-Input AND Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

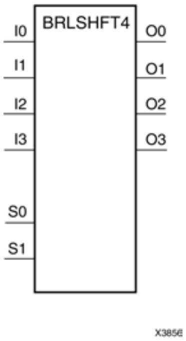
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

BRLSHFT4

Macro: 4-Bit Barrel Shifter



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 4-bit barrel shifter that can rotate four inputs (I3 : I0) up to four places. The control inputs (S1 and S0) determine the number of positions, from one to four, that the data is rotated. The four outputs (O3 : O0) reflect the shifted data inputs.

Logic Table

Inputs						**Outputs**			
S1	**S0**	**I0**	**I1**	**I2**	**I3**	**O0**	**O1**	**O2**	**O3**
0	0	a	b	c	d	a	b	c	d
0	1	a	b	c	d	b	c	d	a
1	0	a	b	c	d	c	d	a	b
1	1	a	b	c	d	d	a	b	c

Design Entry Method

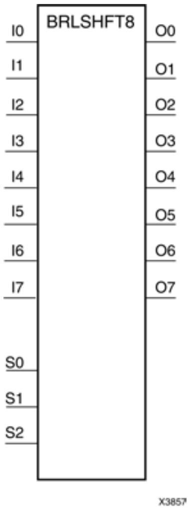
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

BRLSHFT8

Macro: 8-Bit Barrel Shifter



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is an 8-bit barrel shifter, can rotate the eight inputs (I7 : I0) up to eight places. The control inputs (S2 : S0) determine the number of positions, from one to eight, that the data is rotated. The eight outputs (O7 : O0) reflect the shifted data inputs.

Logic Table

Inputs											Outputs							
S2	**S1**	**S0**	**I0**	**I1**	**I2**	**I3**	**I4**	**I5**	**I6**	**I7**	**O0**	**O1**	**O2**	**O3**	**O4**	**O5**	**O6**	**O7**
0	0	0	a	b	c	d	e	f	g	h	a	b	c	d	e	f	g	h
0	0	1	a	b	c	d	e	f	g	h	b	c	d	e	f	g	h	a
0	1	0	a	b	c	d	e	f	g	h	c	d	e	f	g	h	a	b
0	1	1	a	b	c	d	e	f	g	h	d	e	f	g	h	a	b	c
1	0	0	a	b	c	d	e	f	g	h	e	f	g	h	a	b	c	d
1	0	1	a	b	c	d	e	f	g	h	f	g	h	a	b	c	d	e
1	1	0	a	b	c	d	e	f	g	h	g	h	a	b	c	d	e	f
1	1	1	a	b	c	d	e	f	g	h	h	a	b	c	d	e	f	g

Design Entry Method

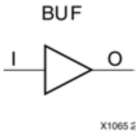
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

BUF

Primitive: General Purpose Buffer



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This is a general-purpose, non-inverting buffer.

This element is not necessary and is removed by the partitioning software (MAP).

Design Entry Method

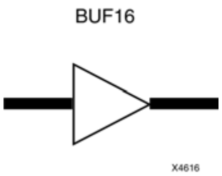
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

BUF16

Macro: 16-Bit General Purpose Buffer



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This is a 16-bit, general purpose, non-inverting buffer. In working with CPLDs, this element is usually removed, unless you inhibit optimization by applying the OPT=OFF attribute to the symbol, or by using the LOGIC_OPT=OFF global attribute.

Design Entry Method

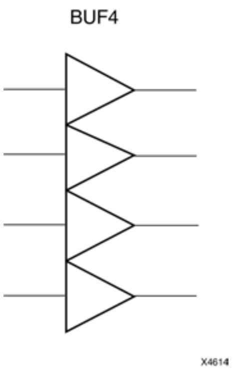
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

BUF4

Macro: 4-Bit General Purpose Buffer



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This is a 4-bit, general purpose, non-inverting buffer. In working with CPLDs, this element is usually removed, unless you inhibit optimization by applying the OPT=OFF attribute to the symbol, or by using the LOGIC_OPT=OFF global attribute.

Design Entry Method

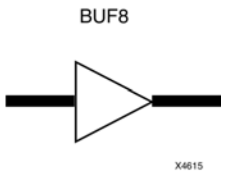
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

BUF8

Macro: 8-Bit General Purpose Buffer



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This is a 8-bit, general purpose, non-inverting buffer. In working with CPLDs, this element is usually removed, unless you inhibit optimization by applying the OPT=OFF attribute to the symbol, or by using the LOGIC_OPT=OFF global attribute.

Design Entry Method

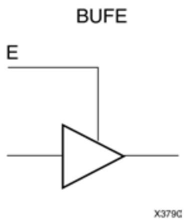
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

BUFE

Primitive: Internal 3-State Buffer with Active High Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™ XPLA3

Introduction

This design element is a single, 3-state buffer with input I and output O, and an active-High output enable (E). When E is High, data on the input of the buffer is transferred to the corresponding output. When E is Low, the output is high impedance (Z state or Off). The outputs of the buffers are connected to horizontal longlines in FPGA architectures.

The outputs of separate symbols for this entity can be tied together to form a bus or a multiplexer. Make sure that only one E is High at any one time. If none of the E inputs is active-High, a "weak-keeper" circuit keeps the output bus from floating but does not guarantee that the bus remains at the last value driven onto it. For certain CPLD devices, output from nets assume the High logic level when all connected BUFE/BUFT buffers are disabled. For FPGA devices, elements need a PULLUP element connected to their output. NGDBuild inserts a PULLUP element if one is not connected.

Logic Table

Inputs		Outputs
E	**I**	**O**
0	X	Z
1	1	1
1	0	0

Design Entry Method

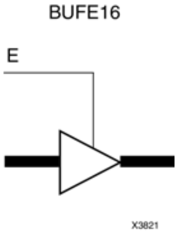
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

BUFE16

Macro: 16-Bit Internal 3-State Buffer with Active High Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™ XPLA3

Introduction

This design element is a multiple 3-state buffer with inputs of I15 : I0 and outputs of O15 : O0 and an active-High output enable (E). When E is High, data on the inputs of the buffers is transferred to the corresponding outputs.

When E is Low, the output is high impedance (Z state or Off). The outputs of the buffers are connected to horizontal longlines in FPGA architectures. The outputs of separate BUFE elements can be tied together to form a bus or a multiplexer. Make sure that only one E is High at any one time. If none of the E inputs is active-High, a "weak-keeper" circuit keeps the output bus from floating but does not guarantee that the bus remains at the last value driven onto it.

Logic Table

Inputs		Outputs
E	**I**	**O**
0	X	Z
1	1	1
1	0	0

Design Entry Method

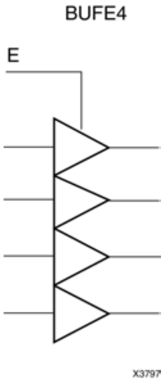
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

BUFE4

Macro: 4-BitInternal 3-State Buffer with Active High Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™ XPLA3

Introduction

This design element is a multiple 3-state buffer with inputs of I3 : I0 and outputs of O3 : O0 and an active-High output enable (E). When E is High, data on the inputs of the buffers is transferred to the corresponding outputs.

When E is Low, the output is high impedance (Z state or Off). The outputs of the buffers are connected to horizontal longlines in FPGA architectures. The outputs of separate BUFE elements can be tied together to form a bus or a multiplexer. Make sure that only one E is High at any one time. If none of the E inputs is active-High, a "weak-keeper" circuit keeps the output bus from floating but does not guarantee that the bus remains at the last value driven onto it.

Logic Table

Inputs		**Outputs**
E	**I**	**O**
0	X	Z
1	1	1
1	0	0

Design Entry Method

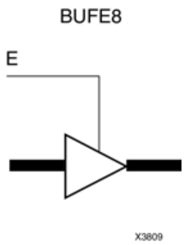
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

BUFE8

Macro: 8-Bit Internal 3-State Buffer with Active High Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™ XPLA3

Introduction

This design element is a multiple 3-state buffer with inputs of I7 : I0 and outputs of O7 : O0 and an active-High output enable (E). When E is High, data on the inputs of the buffers is transferred to the corresponding outputs.

When E is Low, the output is high impedance (Z state or Off). The outputs of the buffers are connected to horizontal longlines in FPGA architectures. The outputs of separate BUFE elements can be tied together to form a bus or a multiplexer. Make sure that only one E is High at any one time. If none of the E inputs is active-High, a “weak-keeper” circuit keeps the output bus from floating but does not guarantee that the bus remains at the last value driven onto it.

Logic Table

Inputs		Outputs
E	**I**	**O**
0	X	Z
1	1	1
1	0	0

Design Entry Method

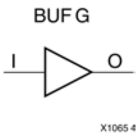
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

BUFG

Primitive: Global Clock Buffer



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a high-fanout buffer that connects signals to the global routing resources for low skew distribution of the signal. BUFGs are typically used on clock nets as well other high fanout nets like sets/resets and clock enables.

Port Descriptions

Port	Type	Width	Function
I	Input	1	Clock buffer input
O	Output	1	Clock buffer output

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- BUFG: Global Clock Buffer
--       Virtex-6
-- Xilinx HDL Libraries Guide, version 11.2

BUFG_inst : BUFG
generic map (
)
port map (
   O => O, -- 1-bit Clock buffer output
   I => I  -- 1-bit Clock buffer input
);

-- End of BUFG_inst instantiation
```

Verilog Instantiation Template

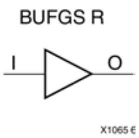
```
// BUFG: Global Clock Buffer (source by an internal signal)
//       All FPGAs
// Xilinx HDL Libraries Guide, version 11.2

BUFG BUFG_inst (
   .O(O),      // Clock buffer output
   .I(I)       // Clock buffer input
);

// End of BUFG_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate EDK documentation.

BUFGSR

Primitive: Global Set/Reset Input Buffer



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element distributes Global Set/Reset (GSR) signals throughout selected flip-flops of an XC9500/XV/XL, CoolRunner™ XPLA3, or CoolRunner™-II device. Global Set/Reset (GSR) control pins are available on these CPLD devices. Consult device data sheets for availability.

This design element always acts as an input buffer. To use it in a schematic, connect the input of the design element symbol to an IPAD or an IOPAD representing the GSR signal source. GSR signals generated on-chip must be passed through an OBUF-type buffer before they are connected to the design element.

For Global Set/Reset (GSR) control, the output of the design element normally connects to the CLR or PRE input of a flip-flop symbol, like FDCP, or any registered symbol with asynchronous clear or preset. The Global Set/Reset (GSR) control signal may pass through an inverter to perform an active-low set/reset. The output of the design element may also be used as an ordinary input signal to other logic elsewhere in the design. This design element can control any number of flip-flops in a design.

Design Entry Method

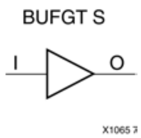
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

BUFGTS

Primitive: Global 3-State Input Buffer



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element distributes global output-enable signals throughout the output pad drivers of CPLD devices. Global Three-State (GTS) control pins are available on these CPLD devices. Consult device data sheets for availability.

This element always acts as an input buffer. To use it in a schematic, connect the input of the BUFGTS symbol to an IPAD or an IOPAD representing the GTS signal source. GTS signals generated on-chip must be passed through an OBUF-type buffer before they are connected to this element.

For global 3-state control, the output of this element normally connects to the E input of a 3-state output buffer symbol, OBUFE. The global 3-state control signal may pass through an inverter or control an OBUFT symbol to perform an active-low output-enable. The same 3-state control signal may even be used both inverted and non-inverted to enable alternate groups of device outputs. The output of BUFGTS may also be used as an ordinary input signal to other logic elsewhere in the design. Each BUFGTS can control any number of output buffers in a design.

Design Entry Method

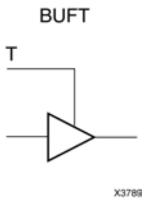
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

BUFT

Primitive: Internal 3-State Buffer with Active Low Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™ XPLA3

Introduction

This design element is a single 3-state buffer with input I and an output of O and active-Low output enable (T). When T is Low, data on the input of the buffer is transferred to the corresponding output. When T is High, the output is high impedance (Z state or off). The output of the buffer is connected to a horizontal longline in FPGA architectures.

The output of separate BUFT symbols can be tied together to form a bus or a multiplexer. Make sure that only one T is Low at one time. For CPLD devices, BUFT output nets assume the High logic level when all connected BUFE/BUFT buffers are disabled. For FPGAs, when all BUFTs on a net are disabled, the net is High. For correct simulation of this effect, a PULLUP element must be connected to the net. NGDBuild inserts a PULLUP element if one is not connected so that back-annotation simulation reflects the true state of the device.

Logic Table

Inputs		Outputs
T	**I**	**O**
1	X	Z
0	1	1
0	0	0

Design Entry Method

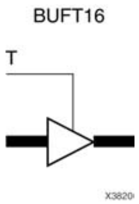
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

BUFT16

Macro: 16-Bit Internal 3-State Buffers with Active Low Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™ XPLA3

Introduction

This design element is a multiple 3-state buffer with inputs I15:I0 and outputs O15:O0 and active-Low output enable (T). When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (Z state or off). The outputs of the buffers are connected to horizontal longlines in FPGA architectures.

The output of separate BUFT symbols can be tied together to form a bus or a multiplexer. Make sure that only one T is Low at one time. For CPLD devices, BUFT output nets assume the High logic level when all connected BUFE/BUFT buffers are disabled. For FPGAs, when all BUFTs on a net are disabled, the net is High. For correct simulation of this effect, a PULLUP element must be connected to the net. NGDBuild inserts a PULLUP element if one is not connected so that back-annotation simulation reflects the true state of the device.

Logic Table

Inputs		Outputs
T	**I**	**O**
1	X	Z
0	1	1
0	0	0

Design Entry Method

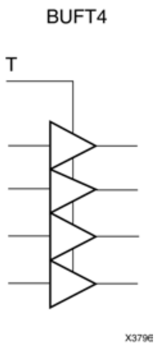
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

BUFT4

Macro: 4-Bit Internal 3-State Buffers with Active Low Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™ XPLA3

Introduction

This design element is a multiple 3-state buffer with inputs I3:I0 and outputs O3:O0 and active-Low output enable (T). When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (Z state or off). The outputs of the buffers are connected to horizontal longlines in FPGA architectures.

The output of separate BUFT symbols can be tied together to form a bus or a multiplexer. Make sure that only one T is Low at one time. For CPLD devices, BUFT output nets assume the High logic level when all connected BUFE/BUFT buffers are disabled. For FPGAs, when all BUFTs on a net are disabled, the net is High. For correct simulation of this effect, a PULLUP element must be connected to the net. NGDBuild inserts a PULLUP element if one is not connected so that back-annotation simulation reflects the true state of the device.

Logic Table

Inputs		Outputs
T	**I**	**O**
1	X	Z
0	1	1
0	0	0

Design Entry Method

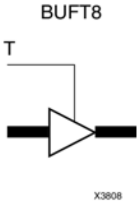
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

BUFT8

Macro: 8-Bit Internal 3-State Buffers with Active Low Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™ XPLA3

Introduction

This design element is a multiple 3-state buffer with inputs I7:I0 and outputs O7:O0 and active-Low output enable (T). When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (Z state or off). The outputs of the buffers are connected to horizontal longlines in FPGA architectures.

The output of separate BUFT symbols can be tied together to form a bus or a multiplexer. Make sure that only one T is Low at one time. For CPLD devices, BUFT output nets assume the High logic level when all connected BUFE/BUFT buffers are disabled. For FPGAs, when all BUFTs on a net are disabled, the net is High. For correct simulation of this effect, a PULLUP element must be connected to the net. NGDBuild inserts a PULLUP element if one is not connected so that back-annotation simulation reflects the true state of the device.

Logic Table

Inputs		Outputs
T	**I**	**O**
1	X	Z
0	1	1
0	0	0

Design Entry Method

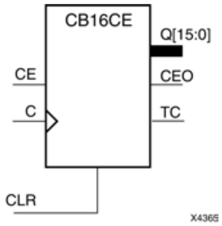
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CB16CE

Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is an asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			**Outputs**		
CLR	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE					

Design Entry Method

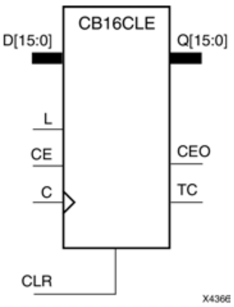
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CB16CLE

Macro: 16-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This element is a synchronously loadable, asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					Outputs		
CLR	**L**	**CE**	**C**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE							

Design Entry Method

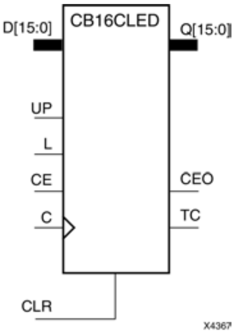
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CB16CLED

Macro: 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to- High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n (t_{CE-TC}), where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

For CPLD parts, see “CB2X1”, “CB4X1”, “CB8X1”, “CB16X1” for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs		
CLR	**L**	**CE**	**C**	**UP**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO
z = bit width - 1 TC = (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) + (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) CEO = TC•CE								

Design Entry Method

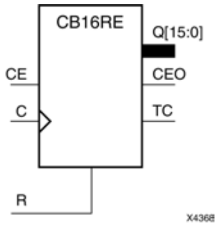
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CB16RE

Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronous, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			**Outputs**		
R	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	↑	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0) CEO = TC•CE					

Design Entry Method

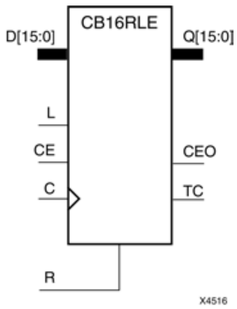
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CB16RLE

Macro: 16-Bit Loadable Cascadable Binary Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronous, loadable, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock (C) transition.

The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of CE. The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High. The CEO output is High when all Q outputs and CE are High to allow direct cascading of counters.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					Outputs		
R	**L**	**CE**	**C**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	↑	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE							

Design Entry Method

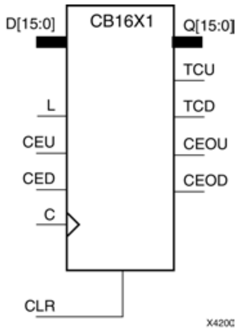
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CB16X1

Macro: 16-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronously loadable, asynchronously clearable, bidirectional binary counter. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading.

The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, clock enable outputs CEOU and CEOD go to Low and High, respectively, independent of clock transitions. The data on the D inputs loads into the counter on the Low-to-High clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

The Q outputs increment when CEU is High, provided CLR and L are Low, during the Low-to-High clock transition. The Q outputs decrement when CED is High, provided CLR and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, connect the CEOU and CEOD outputs of each counter directly to the CEU and CED inputs, respectively, of the next stage. Connect the clock, L, and CLR inputs in parallel.

The maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

The counter is initialized to zero (TCU Low and TCD High) when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs				
CLR	**L**	**CEU**	**CED**	**C**	**Dz-D0**	**Qz-Q0**	**TCU**	**TCD**	**CEOU**	**CEOD**
1	X	X	X	X	X	0	0	1	0	CEOD
0	1	X	X	↑	Dn	Dn	TCU	TCD	CEOU	CEOD
0	0	0	0	X	X	No Change	No Change	No Change	0	0
0	0	1	0	↑	X	Inc	TCU	TCD	CEOU	0
0	0	0	1	↑	X	Dec	TCU	TCD	0	CEOD
0	0	1	1	↑	X	Inc	TCU	TCD	Invalid	Invalid
z = bit width - 1 TCU = Qz•Q(z-1)•Q(z-2)•...•Q0 TCD = Qz•Q(z-1)•Q(z-2)•...•Q0 CEOU = TCU•CEU CEOD = TCD•CED										

Design Entry Method

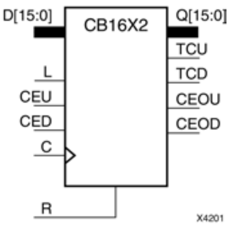
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CB16X2

Macro: 16-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Synchro-nous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronous, loadable, resettable, bidirectional binary counter. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading in CPLD architectures.

The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, and clock enable outputs CEOU and CEOD go to Low and High, respectively, on the Low-to-High clock (C) transition. The data on the D inputs loads into the counter on the Low-to-High clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

All Q outputs increment when CEU is High, provided R and L are Low during the Low-to-High clock transition. All Q outputs decrement when CED is High, provided R and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, the CEOU and CEOD outputs of each counter are, respectively, connected directly to the CEU and CED inputs of the next stage. The C, L, and R inputs are connected in parallel.

The maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

The counter is initialized to zero (TCU Low and TCD High) when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs				
R	L	CEU	CED	C	Dz-D0	Qz-Q0	TCU	TCD	CEOU	CEOD
1	X	X	X	↑	X	0	0	1	0	CEOD
0	1	X	X	↑	Dn	Dn	TCU	TCD	CEOU	CEOD
0	0	0	0	X	X	No Chg	No Chg	No Chg	0	0
0	0	1	0	↑	X	Inc	TCU	TCD	CEOU	0
0	0	0	1	↑	X	Dec	TCU	TCD	0	CEOD
0	0	1	1	↑	X	Inc	TCU	TCD	Invalid	Invalid
z = bit width - 1 TCU = QzQ(z-1)Q(z-2)...Q0 TCD = QzQ(z-1)Q(z-2)...Q0 CEOU = TCUCEU CEOD = TCDCED										

Design Entry Method

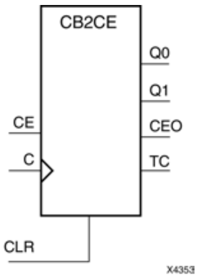
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CB2CE

Macro: 2-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is an asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			**Outputs**		
CLR	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE					

Design Entry Method

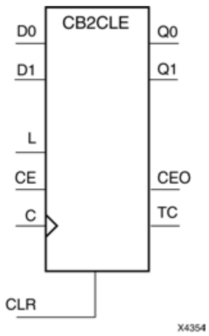
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CB2CLE

Macro: 2-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This element is a synchronously loadable, asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					**Outputs**		
CLR	**L**	**CE**	**C**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
z = bit width - 1							
TC = Qz•Q(z-1)•Q(z-2)•...•Q0							

Inputs					Outputs		
CLR	**L**	**CE**	**C**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
CEO = TC•CE							

Design Entry Method

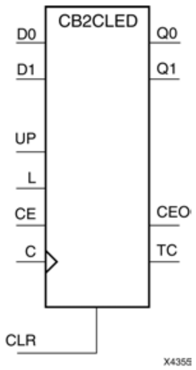
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CB2CLED

Macro: 2-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to- High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

For CPLD parts, see “CB2X1”, “CB4X1”, “CB8X1”, “CB16X1” for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs		
CLR	**L**	**CE**	**C**	**UP**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO
z = bit width - 1 TC = (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) + (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) CEO = TC•CE								

Design Entry Method

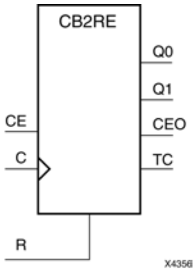
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CB2RE

Macro: 2-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronous, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			**Outputs**		
R	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	↑	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0) CEO = TC•CE					

Design Entry Method

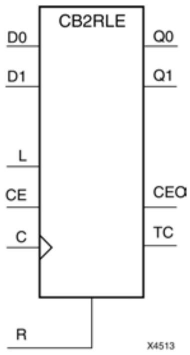
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CB2RLE

Macro: 2-Bit Loadable Cascadable Binary Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronous, loadable, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock (C) transition.

The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of CE. The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High. The CEO output is High when all Q outputs and CE are High to allow direct cascading of counters.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n (t_{CE-TC}), where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					Outputs		
R	**L**	**CE**	**C**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	↑	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE							

Design Entry Method

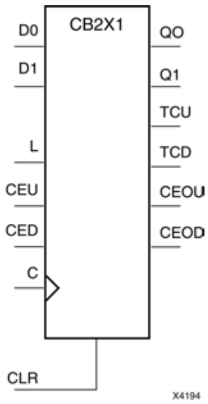
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CB2X1

Macro: 2-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronously loadable, asynchronously clearable, bidirectional binary counter. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading.

The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, clock enable outputs CEOU and CEOD go to Low and High, respectively, independent of clock transitions. The data on the D inputs loads into the counter on the Low-to-High clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

The Q outputs increment when CEU is High, provided CLR and L are Low, during the Low-to-High clock transition. The Q outputs decrement when CED is High, provided CLR and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, connect the CEOU and CEOD outputs of each counter directly to the CEU and CED inputs, respectively, of the next stage. Connect the clock, L, and CLR inputs in parallel.

The maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

The counter is initialized to zero (TCU Low and TCD High) when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs				
CLR	**L**	**CEU**	**CED**	**C**	**Dz-D0**	**Qz-Q0**	**TCU**	**TCD**	**CEOU**	**CEOD**
1	X	X	X	X	X	0	0	1	0	CEOD
0	1	X	X	↑	Dn	Dn	TCU	TCD	CEOU	CEOD
0	0	0	0	X	X	No Change	No Change	No Change	0	0
0	0	1	0	↑	X	Inc	TCU	TCD	CEOU	0
0	0	0	1	↑	X	Dec	TCU	TCD	0	CEOD
0	0	1	1	↑	X	Inc	TCU	TCD	Invalid	Invalid
z = bit width - 1										
TCU = Qz•Q(z-1)•Q(z-2)•...•Q0										
TCD = Qz•Q(z-1)•Q(z-2)•...•Q0										
CEOU = TCU•CEU										
CEOD = TCD•CED										

Design Entry Method

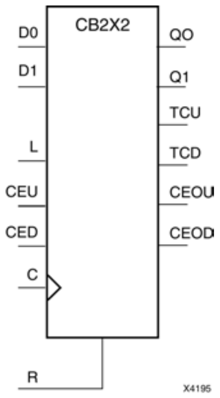
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CB2X2

Macro: 2-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronous, loadable, resettable, bidirectional binary counter. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading in CPLD architectures.

The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, and clock enable outputs CEOU and CEOD go to Low and High, respectively, on the Low-to-High clock (C) transition. The data on the D inputs loads into the counter on the Low-to-High clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

All Q outputs increment when CEU is High, provided R and L are Low during the Low-to-High clock transition. All Q outputs decrement when CED is High, provided R and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, the CEOU and CEOD outputs of each counter are, respectively, connected directly to the CEU and CED inputs of the next stage. The C, L, and R inputs are connected in parallel.

The maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

The counter is initialized to zero (TCU Low and TCD High) when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs				
R	**L**	**CEU**	**CED**	**C**	**Dz-D0**	**Qz-Q0**	**TCU**	**TCD**	**CEOU**	**CEOD**
1	X	X	X	↑	X	0	0	1	0	CEOD
0	1	X	X	↑	Dn	Dn	TCU	TCD	CEOU	CEOD
0	0	0	0	X	X	No Chg	No Chg	No Chg	0	0
0	0	1	0	↑	X	Inc	TCU	TCD	CEOU	0
0	0	0	1	↑	X	Dec	TCU	TCD	0	CEOD
0	0	1	1	↑	X	Inc	TCU	TCD	Invalid	Invalid
z = bit width - 1 TCU = QzQ(z-1)Q(z-2)...Q0 TCD = QzQ(z-1)Q(z-2)...Q0 CEOU = TCUCEU CEOD = TCDCED										

Design Entry Method

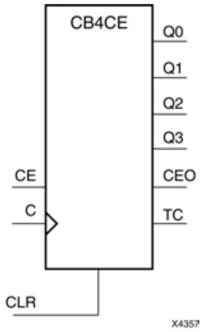
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CB4CE

Macro: 4-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is an asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			Outputs		
CLR	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE					

Design Entry Method

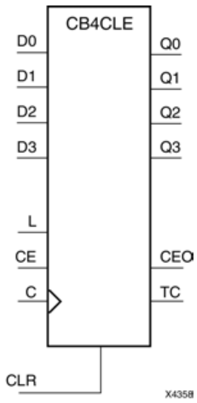
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CB4CLE

Macro: 4-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This element is a synchronously loadable, asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n (t_{CE-TC}), where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					Outputs		
CLR	**L**	**CE**	**C**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE							

Design Entry Method

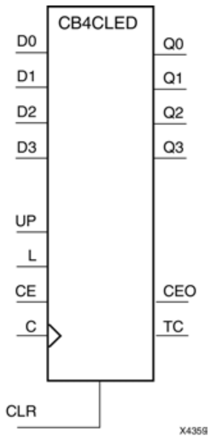
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CB4CLED

Macro: 4-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to- High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

For CPLD parts, see “CB2X1”, “CB4X1”, “CB8X1”, “CB16X1” for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs		
CLR	**L**	**CE**	**C**	**UP**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO
z = bit width - 1								
TC = (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) + (Qz•Q(z-1)•Q(z-2)•...•Q0•UP)								
CEO = TC•CE								

Design Entry Method

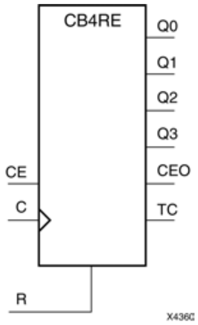
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CB4RE

Macro: 4-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronous, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			Outputs		
R	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	↑	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0) CEO = TC•CE					

Design Entry Method

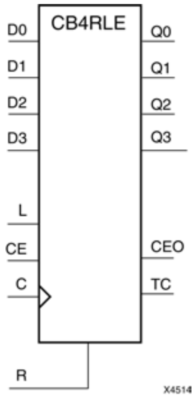
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CB4RLE

Macro: 4-Bit Loadable Cascadable Binary Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronous, loadable, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock (C) transition.

The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of CE. The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High. The CEO output is High when all Q outputs and CE are High to allow direct cascading of counters.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n (t_{CE-TC}), where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					Outputs		
R	**L**	**CE**	**C**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	↑	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE							

Design Entry Method

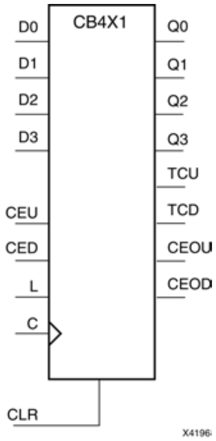
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CB4X1

Macro: 4-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronously loadable, asynchronously clearable, bidirectional binary counter. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading.

The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, clock enable outputs CEOU and CEOD go to Low and High, respectively, independent of clock transitions. The data on the D inputs loads into the counter on the Low-to-High clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

The Q outputs increment when CEU is High, provided CLR and L are Low, during the Low-to-High clock transition. The Q outputs decrement when CED is High, provided CLR and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, connect the CEOU and CEOD outputs of each counter directly to the CEU and CED inputs, respectively, of the next stage. Connect the clock, L, and CLR inputs in parallel.

The maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

The counter is initialized to zero (TCU Low and TCD High) when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						**Outputs**				
CLR	**L**	**CEU**	**CED**	**C**	**Dz-D0**	**Qz-Q0**	**TCU**	**TCD**	**CEOU**	**CEOD**
1	X	X	X	X	X	0	0	1	0	CEOD
0	1	X	X	↑	Dn	Dn	TCU	TCD	CEOU	CEOD
0	0	0	0	X	X	No Change	No Change	No Change	0	0
0	0	1	0	↑	X	Inc	TCU	TCD	CEOU	0
0	0	0	1	↑	X	Dec	TCU	TCD	0	CEOD
0	0	1	1	↑	X	Inc	TCU	TCD	Invalid	Invalid

z = bit width - 1

TCU = Qz•Q(z-1)•Q(z-2)•...•Q0

TCD = Qz•Q(z-1)•Q(z-2)•...•Q0

CEOU = TCU•CEU

CEOD = TCD•CED

Design Entry Method

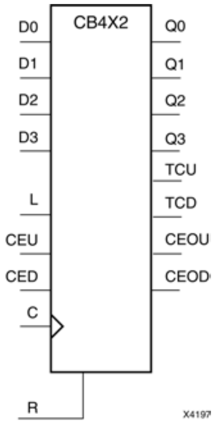
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CB4X2

Macro: 4-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronous, loadable, resettable, bidirectional binary counter. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading in CPLD architectures.

The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, and clock enable outputs CEOU and CEOD go to Low and High, respectively, on the Low-to-High clock (C) transition. The data on the D inputs loads into the counter on the Low-to-High clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

All Q outputs increment when CEU is High, provided R and L are Low during the Low-to-High clock transition. All Q outputs decrement when CED is High, provided R and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, the CEOU and CEOD outputs of each counter are, respectively, connected directly to the CEU and CED inputs of the next stage. The C, L, and R inputs are connected in parallel.

The maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

The counter is initialized to zero (TCU Low and TCD High) when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						**Outputs**				
R	**L**	**CEU**	**CED**	**C**	**Dz-D0**	**Qz-Q0**	**TCU**	**TCD**	**CEOU**	**CEOD**
1	X	X	X	↑	X	0	0	1	0	CEOD
0	1	X	X	↑	Dn	Dn	TCU	TCD	CEOU	CEOD
0	0	0	0	X	X	No Chg	No Chg	No Chg	0	0
0	0	1	0	↑	X	Inc	TCU	TCD	CEOU	0
0	0	0	1	↑	X	Dec	TCU	TCD	0	CEOD
0	0	1	1	↑	X	Inc	TCU	TCD	Invalid	Invalid

z = bit width - 1

TCU = QzQ(z-1)Q(z-2)...Q0

TCD = QzQ(z-1)Q(z-2)...Q0

CEOU = TCUCEU

CEOD = TCDCED

Design Entry Method

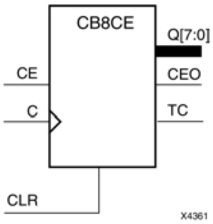
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CB8CE

Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is an asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{\text{CE-TC}}$), where n is the number of stages and the time $t_{\text{CE-TC}}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			Outputs		
CLR	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE					

Design Entry Method

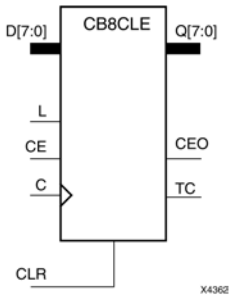
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CB8CLE

Macro: 8-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This element is a synchronously loadable, asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					**Outputs**		
CLR	**L**	**CE**	**C**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
z = bit width - 1							
TC = Qz•Q(z-1)•Q(z-2)•...•Q0							
CEO = TC•CE							

Design Entry Method

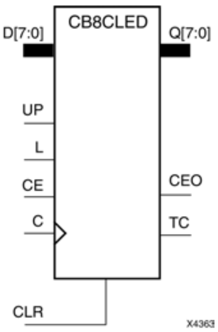
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CB8CLED

Macro: 8-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to- High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

For CPLD parts, see "CB2X1", "CB4X1", "CB8X1", "CB16X1" for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs		
CLR	**L**	**CE**	**C**	**UP**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO
z = bit width - 1 TC = (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) + (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) CEO = TC•CE								

Design Entry Method

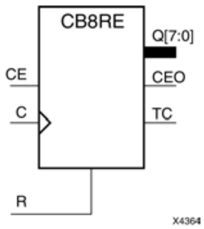
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CB8RE

Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronous, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			Outputs		
R	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	↑	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1					
TC = Qz•Q(z-1)•Q(z-2)•...•Q0)					
CEO = TC•CE					

Design Entry Method

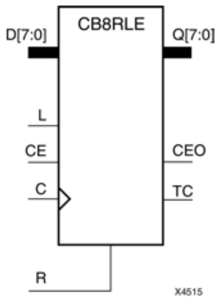
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CB8RLE

Macro: 8-Bit Loadable Cascadable Binary Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronous, loadable, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock (C) transition.

The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of CE. The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High. The CEO output is High when all Q outputs and CE are High to allow direct cascading of counters.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					**Outputs**		
R	**L**	**CE**	**C**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	↑	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE							

Design Entry Method

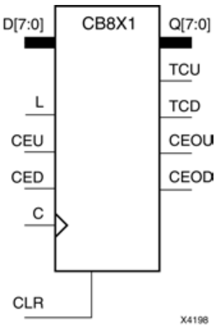
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CB8X1

Macro: 8-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronously loadable, asynchronously clearable, bidirectional binary counter. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading.

The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, clock enable outputs CEOU and CEOD go to Low and High, respectively, independent of clock transitions. The data on the D inputs loads into the counter on the Low-to-High clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

The Q outputs increment when CEU is High, provided CLR and L are Low, during the Low-to-High clock transition. The Q outputs decrement when CED is High, provided CLR and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, connect the CEOU and CEOD outputs of each counter directly to the CEU and CED inputs, respectively, of the next stage. Connect the clock, L, and CLR inputs in parallel.

The maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

The counter is initialized to zero (TCU Low and TCD High) when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs				
CLR	**L**	**CEU**	**CED**	**C**	**Dz-D0**	**Qz-Q0**	**TCU**	**TCD**	**CEOU**	**CEOD**
1	X	X	X	X	X	0	0	1	0	CEOD
0	1	X	X	↑	Dn	Dn	TCU	TCD	CEOU	CEOD
0	0	0	0	X	X	No Change	No Change	No Change	0	0
0	0	1	0	↑	X	Inc	TCU	TCD	CEOU	0
0	0	0	1	↑	X	Dec	TCU	TCD	0	CEOD
0	0	1	1	↑	X	Inc	TCU	TCD	Invalid	Invalid
z = bit width - 1 TCU = Qz•Q(z-1)•Q(z-2)•...•Q0 TCD = Qz•Q(z-1)•Q(z-2)•...•Q0 CEOU = TCU•CEU CEOD = TCD•CED										

Design Entry Method

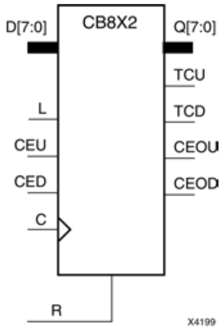
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CB8X2

Macro: 8-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronous, loadable, resettable, bidirectional binary counter. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading in CPLD architectures.

The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, and clock enable outputs CEOU and CEOD go to Low and High, respectively, on the Low-to-High clock (C) transition. The data on the D inputs loads into the counter on the Low-to-High clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

All Q outputs increment when CEU is High, provided R and L are Low during the Low-to-High clock transition. All Q outputs decrement when CED is High, provided R and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, the CEOU and CEOD outputs of each counter are, respectively, connected directly to the CEU and CED inputs of the next stage. The C, L, and R inputs are connected in parallel.

The maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

The counter is initialized to zero (TCU Low and TCD High) when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs				
R	L	CEU	CED	C	Dz-D0	Qz-Q0	TCU	TCD	CEOU	CEOD
1	X	X	X	↑	X	0	0	1	0	CEOD
0	1	X	X	↑	Dn	Dn	TCU	TCD	CEOU	CEOD
0	0	0	0	X	X	No Chg	No Chg	No Chg	0	0
0	0	1	0	↑	X	Inc	TCU	TCD	CEOU	0
0	0	0	1	↑	X	Dec	TCU	TCD	0	CEOD
0	0	1	1	↑	X	Inc	TCU	TCD	Invalid	Invalid
z = bit width - 1 TCU = QzQ(z-1)Q(z-2)...Q0 TCD = QzQ(z-1)Q(z-2)...Q0 CEOU = TCUCEU CEOD = TCDCED										

Design Entry Method

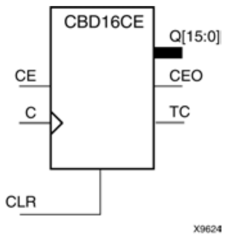
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CBD16CE

Macro: 16-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This element is an asynchronously clearable, cascadable dual edge triggered binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			**Outputs**		
CLR	**CE**	**C**	**Qz : Q0**	**TC**	**CEO**
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
0	1	↓	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE					

Design Entry Method

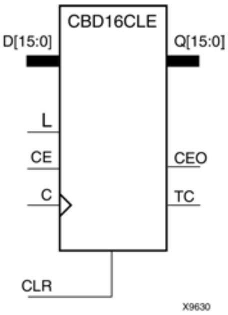
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CBD16CLE

Macro: 16-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This is a synchronously loadable, asynchronously clearable, cascadable dual edge triggered binary counters. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High and High-to-Low clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					Outputs		
CLR	**L**	**CE**	**C**	**Dz : D0**	**Qz : Q0**	**TC**	**CEO**
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	1	X	↓	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
0	0	1	↓	X	Inc	TC	CEO

Inputs					Outputs		
CLR	L	CE	C	Dz : D0	Qz : Q0	TC	CEO
z = bit width - 1							
TC = Qz•Q(z-1)•Q(z-2)•...•Q0							
CEO = TC•CE							

Design Entry Method

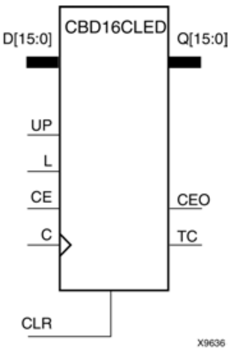
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CBD16CLED

Macro: 16-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional dual edge triggered binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High and High-to-Low clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

See CB2X1, CB4X1, CB8X1, CB16X1 for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs		
CLR	**L**	**CE**	**C**	**UP**	**Dz : D0**	**Qz : Q0**	**TC**	**CEO**
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	1	X	↓	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↓	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO
0	0	1	↓	0	X	Dec	TC	CEO

z = bit width - 1

TC = (QzQ(z-1)Q(z-2)...Q0UP) + (QzQ(z-1)Q(z-2)...Q0UP)

CEO = TCCE

Design Entry Method

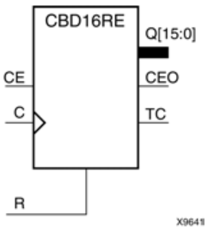
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CBD16RE

Macro: 16-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a synchronous, resettable, cascadable dual edge triggered binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero during the Low-to-High or High-to-Low clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n (t_{CE-TC}), where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			**Outputs**		
R	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	↑	0	0	0
1	X	↓	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
0	1	↓	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0) CEO = TC•CE					

Design Entry Method

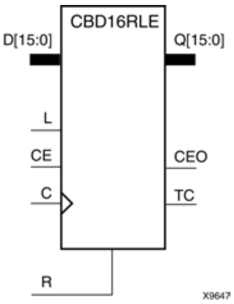
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CBD16RLE

Macro: 16-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a synchronous, loadable, resettable, cascadable dual edge triggered binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) outputs to Low on the Low-to-High or High-to-Low clock (C) transition.

The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High and High-to-Low clock (C) transition, independent of the state of CE. The Q outputs increment when CE is High during the Low-to-High and High-to-Low clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High. The CEO output is High when all Q outputs and CE are High to allow direct cascading of counters.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n (t_{CE-TC}), where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					Outputs		
R	**L**	**CE**	**C**	**Dz : D0**	**Qz : Q0**	**TC**	**CEO**
1	X	X	↑	X	0	0	0
1	X	X	↓	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	1	X	↓	Dn	Dn	TC	CEO

Inputs					Outputs		
R	L	CE	C	Dz : D0	Qz : Q0	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
0	0	1	↓	X	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE							

Design Entry Method

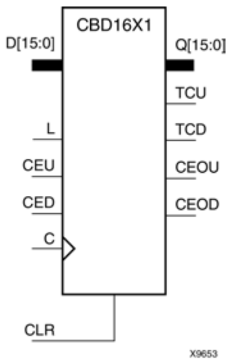
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CBD16X1

Macro: 16-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a synchronously loadable, asynchronously clearable, bidirectional dual edge triggered binary counters. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high speed cascading.

The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, clock enable outputs CEOU and CEOD go to Low and High, respectively, independent of clock transitions. The data on the D inputs loads into the counter on the Low-to-High and High-to-Low clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

The Q outputs increment when CEU is High, provided CLR and L are Low, during the Low-to-High and High-to-Low clock transition. The Q outputs decrement when CED is High, provided CLR and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, the CEOU and CEOD outputs of each counter are connected directly to the CEU and CED inputs, respectively, of the next stage. The clock, L, and CLR inputs are connected in parallel.

The maximum clocking frequency of these counters is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs				
CLR	L	CEU	CED	C	Dz–D0	Qz–Q0	TCU	TCD	CEOU	CEOD
1	X	X	X	X	X	0	0	1	0	CEOD
0	1	X	X	↑	Dn	Dn	TCU	TCD	CEOU	CEOD
0	1	X	X	↓	Dn	Dn	TCU	TCD	CEOU	CEOD
0	0	0	0	X	X	No Change	No Change	No Change	0	0
0	0	1	0	↑	X	Inc	TCU	TCD	CEOU	0
0	0	1	0	↓	X	Inc	TCU	TCD	CEOU	0
0	0	0	1	↑	X	Dec	TCU	TCD	0	CEOD
0	0	0	1	↓	X	Dec	TCU	TCD	0	CEOD
0	0	1	1	↑	X	Inc	TCU	TCD	Invalid	Invalid
0	0	1	1	↓	X	Inc	TCU	TCD	Invalid	Invalid
z = bit width - 1 TCU = Qz•Q(z-1)•Q(z-2)•...•Q0 TCD = Qz•Q(z-1)•Q(z-2)•...•Q0 CEOU = TCU•CEU CEOD = TCD•CED										

Design Entry Method

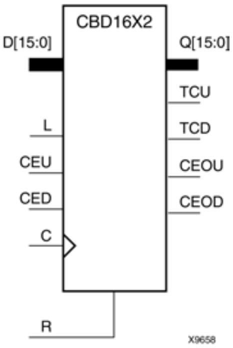
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CBD16X2

Macro: 16-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a synchronous, loadable, resettable, bidirectional dual edge triggered binary counter. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading.

The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, and clock enable outputs CEOU and CEOD go to Low and High, respectively, on the Low-to-High and High-to-Low clock (C) transition. The data on the D inputs loads into the counter on the Low-to-High and High-to-Low clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

All Q outputs increment when CEU is High, provided R and L are Low during the Low-to-High and High-to-Low clock transition. All Q outputs decrement when CED is High, provided R and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, the CEOU and CEOD outputs of each counter are, respectively, connected directly to the CEU and CED inputs of the next stage. The C, L, and R inputs are connected in parallel.

The maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs				
R	**L**	**CEU**	**CED**	**C**	**Dz : D0**	**Qz : Q0**	**TCU**	**TCD**	**CEOU**	**CEOD**
1	X	X	X	↑	X	0	0	1	0	CEOD
1	X	X	X	↓	X	0	0	1	0	CEOD
0	1	X	X	↑	Dn	Dn	TCU	TCD	CEOU	CEOD
0	1	X	X	↓	Dn	Dn	TCU	TCD	CEOU	CEOD
0	0	0	0	X	X	No Change	No Change	No Change	0	0
0	0	1	0	↑	X	Inc	TCU	TCD	CEOU	0
0	0	1	0	↓	X	Inc	TCU	TCD	CEOU	0
0	0	0	1	↑	X	Dec	TCU	TCD	0	CEOD
0	0	0	1	↓	X	Dec	TCU	TCD	0	CEOD
0	0	1	1	↑	X	Inc	TCU	TCD	Invalid	Invalid
0	0	1	1	↓	X	Inc	TCU	TCD	Invalid	Invalid
z = bit width - 1 TCU = Qz•Q(z-1)•Q(z-2)•...•Q0 TCD = Qz•Q(z-1)•Q(z-2)•...•Q0 CEOU = TCU•CEU CEOD = TCD•CED										

Design Entry Method

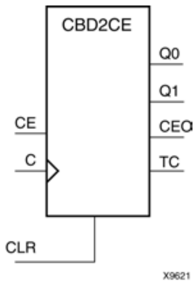
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CBD2CE

Macro: 2-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This element is an asynchronously clearable, cascadable dual edge triggered binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			**Outputs**		
CLR	**CE**	**C**	**Qz : Q0**	**TC**	**CEO**
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
0	1	↓	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE					

Design Entry Method

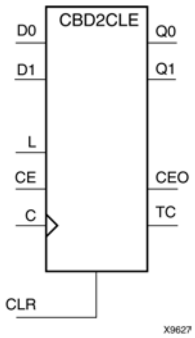
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CBD2CLE

Macro: 2-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This is a synchronously loadable, asynchronously clearable, cascadable dual edge triggered binary counters. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High and High-to-Low clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					Outputs		
CLR	**L**	**CE**	**C**	**Dz : D0**	**Qz : Q0**	**TC**	**CEO**
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	1	X	↓	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
0	0	1	↓	X	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE							

Design Entry Method

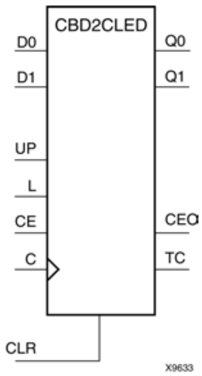
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CBD2CLED

Macro: 2-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional dual edge triggered binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High and High-to-Low clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n (t_{CE-TC}), where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

See CB2X1, CB4X1, CB8X1, CB16X1 for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs		
CLR	**L**	**CE**	**C**	**UP**	**Dz : D0**	**Qz : Q0**	**TC**	**CEO**
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	1	X	↓	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↓	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO
0	0	1	↓	0	X	Dec	TC	CEO

z = bit width - 1

TC = (QzQ(z-1)Q(z-2)...Q0UP) + (QzQ(z-1)Q(z-2)...Q0UP)

CEO = TCCE

Design Entry Method

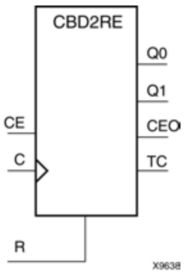
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CBD2RE

Macro: 2-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a synchronous, resettable, cascadable dual edge triggered binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero during the Low-to-High or High-to-Low clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			**Outputs**		
R	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	↑	0	0	0
1	X	↓	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
0	1	↓	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0) CEO = TC•CE					

Design Entry Method

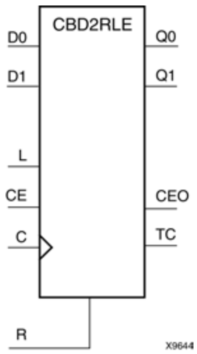
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CBD2RLE

Macro: 2-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a synchronous, loadable, resettable, cascadable dual edge triggered binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) outputs to Low on the Low-to-High or High-to-Low clock (C) transition.

The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High and High-to-Low clock (C) transition, independent of the state of CE. The Q outputs increment when CE is High during the Low-to-High and High-to-Low clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High. The CEO output is High when all Q outputs and CE are High to allow direct cascading of counters.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n (t_{CE-TC}), where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					Outputs		
R	L	CE	C	Dz : D0	Qz : Q0	TC	CEO
1	X	X	↑	X	0	0	0
1	X	X	↓	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	1	X	↓	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
0	0	1	↓	X	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE							

Design Entry Method

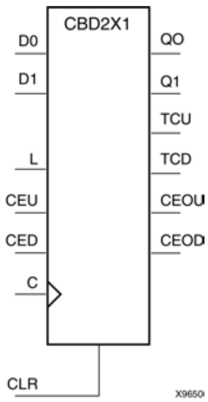
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CBD2X1

Macro: 2-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a synchronously loadable, asynchronously clearable, bidirectional dual edge triggered binary counters. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high speed cascading.

The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, clock enable outputs CEOU and CEOD go to Low and High, respectively, independent of clock transitions. The data on the D inputs loads into the counter on the Low-to-High and High-to-Low clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

The Q outputs increment when CEU is High, provided CLR and L are Low, during the Low-to-High and High-to-Low clock transition. The Q outputs decrement when CED is High, provided CLR and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, the CEOU and CEOD outputs of each counter are connected directly to the CEU and CED inputs, respectively, of the next stage. The clock, L, and CLR inputs are connected in parallel.

The maximum clocking frequency of these counters is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs				
CLR	L	CEU	CED	C	Dz–D0	Qz–Q0	TCU	TCD	CEOU	CEOD
1	X	X	X	X	X	0	0	1	0	CEOD
0	1	X	X	↑	Dn	Dn	TCU	TCD	CEOU	CEOD
0	1	X	X	↓	Dn	Dn	TCU	TCD	CEOU	CEOD
0	0	0	0	X	X	No Change	No Change	No Change	0	0
0	0	1	0	↑	X	Inc	TCU	TCD	CEOU	0
0	0	1	0	↓	X	Inc	TCU	TCD	CEOU	0
0	0	0	1	↑	X	Dec	TCU	TCD	0	CEOD
0	0	0	1	↓	X	Dec	TCU	TCD	0	CEOD
0	0	1	1	↑	X	Inc	TCU	TCD	Invalid	Invalid
0	0	1	1	↓	X	Inc	TCU	TCD	Invalid	Invalid
z = bit width - 1 TCU = Qz•Q(z-1)•Q(z-2)•...•Q0 TCD = Qz•Q(z-1)•Q(z-2)•...•Q0 CEOU = TCU•CEU CEOD = TCD•CED										

Design Entry Method

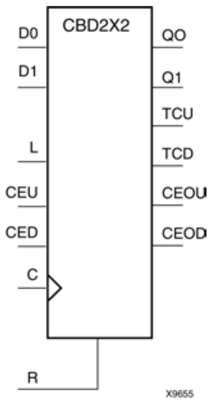
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CBD2X2

Macro: 2-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a synchronous, loadable, resettable, bidirectional dual edge triggered binary counter. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading.

The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, and clock enable outputs CEOU and CEOD go to Low and High, respectively, on the Low-to-High and High-to-Low clock (C) transition. The data on the D inputs loads into the counter on the Low-to-High and High-to-Low clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

All Q outputs increment when CEU is High, provided R and L are Low during the Low-to-High and High-to-Low clock transition. All Q outputs decrement when CED is High, provided R and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, the CEOU and CEOD outputs of each counter are, respectively, connected directly to the CEU and CED inputs of the next stage. The C, L, and R inputs are connected in parallel.

The maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs				
R	L	CEU	CED	C	Dz : D0	Qz : Q0	TCU	TCD	CEOU	CEOD
1	X	X	X	↑	X	0	0	1	0	CEOD
1	X	X	X	↓	X	0	0	1	0	CEOD
0	1	X	X	↑	Dn	Dn	TCU	TCD	CEOU	CEOD
0	1	X	X	↓	Dn	Dn	TCU	TCD	CEOU	CEOD
0	0	0	0	X	X	No Change	No Change	No Change	0	0
0	0	1	0	↑	X	Inc	TCU	TCD	CEOU	0
0	0	1	0	↓	X	Inc	TCU	TCD	CEOU	0
0	0	0	1	↑	X	Dec	TCU	TCD	0	CEOD
0	0	0	1	↓	X	Dec	TCU	TCD	0	CEOD
0	0	1	1	↑	X	Inc	TCU	TCD	Invalid	Invalid
0	0	1	1	↓	X	Inc	TCU	TCD	Invalid	Invalid
z = bit width - 1 TCU = Qz•Q(z-1)•Q(z-2)•...•Q0 TCD = Qz•Q(z-1)•Q(z-2)•...•Q0 CEOU = TCU•CEU CEOD = TCD•CED										

Design Entry Method

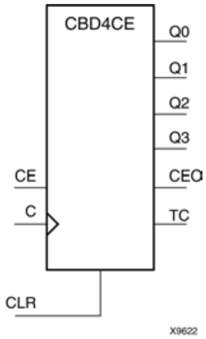
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CBD4CE

Macro: 4-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This element is an asynchronously clearable, cascadable dual edge triggered binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			**Outputs**		
CLR	**CE**	**C**	**Qz : Q0**	**TC**	**CEO**
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
0	1	↓	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE					

Design Entry Method

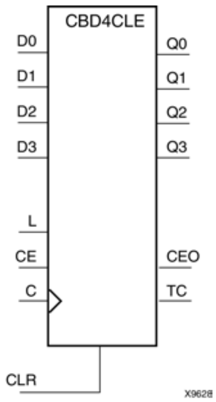
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CBD4CLE

Macro: 4-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This is a synchronously loadable, asynchronously clearable, cascadable dual edge triggered binary counters. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High and High-to-Low clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					Outputs		
CLR	**L**	**CE**	**C**	**Dz : D0**	**Qz : Q0**	**TC**	**CEO**
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	1	X	↓	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
0	0	1	↓	X	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE							

Design Entry Method

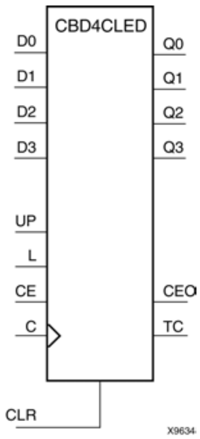
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CBD4CLED

Macro: 4-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional dual edge triggered binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High and High-to-Low clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

See CB2X1, CB4X1, CB8X1, CB16X1 for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs		
CLR	**L**	**CE**	**C**	**UP**	**Dz : D0**	**Qz : Q0**	**TC**	**CEO**
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	1	X	↓	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↓	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO
0	0	1	↓	0	X	Dec	TC	CEO
z = bit width - 1 TC = (QzQ(z-1)Q(z-2)...Q0UP) + (QzQ(z-1)Q(z-2)...Q0UP) CEO = TCCE								

Design Entry Method

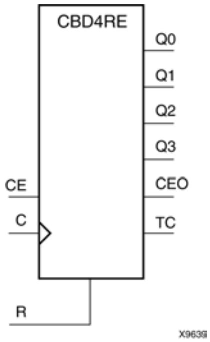
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CBD4RE

Macro: 4-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a synchronous, resettable, cascadable dual edge triggered binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero during the Low-to-High or High-to-Low clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n (t_{CE-TC}), where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			Outputs		
R	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	↑	0	0	0
1	X	↓	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
0	1	↓	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0) CEO = TC•CE					

Design Entry Method

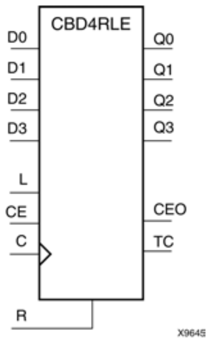
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CBD4RLE

Macro: 4-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a synchronous, loadable, resettable, cascadable dual edge triggered binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) outputs to Low on the Low-to-High or High-to-Low clock (C) transition.

The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High and High-to-Low clock (C) transition, independent of the state of CE. The Q outputs increment when CE is High during the Low-to-High and High-to-Low clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High. The CEO output is High when all Q outputs and CE are High to allow direct cascading of counters.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					Outputs		
R	**L**	**CE**	**C**	**Dz : D0**	**Qz : Q0**	**TC**	**CEO**
1	X	X	↑	X	0	0	0
1	X	X	↓	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	1	X	↓	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
0	0	1	↓	X	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE							

Design Entry Method

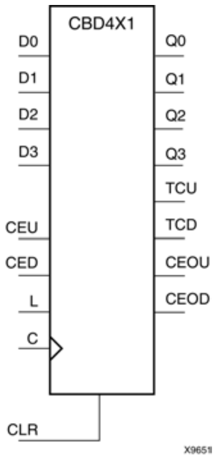
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CBD4X1

Macro: 4-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a synchronously loadable, asynchronously clearable, bidirectional dual edge triggered binary counters. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high speed cascading.

The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, clock enable outputs CEOU and CEOD go to Low and High, respectively, independent of clock transitions. The data on the D inputs loads into the counter on the Low-to-High and High-to-Low clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

The Q outputs increment when CEU is High, provided CLR and L are Low, during the Low-to-High and High-to-Low clock transition. The Q outputs decrement when CED is High, provided CLR and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, the CEOU and CEOD outputs of each counter are connected directly to the CEU and CED inputs, respectively, of the next stage. The clock, L, and CLR inputs are connected in parallel.

The maximum clocking frequency of these counters is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs				
CLR	**L**	**CEU**	**CED**	**C**	**Dz–D0**	**Qz–Q0**	**TCU**	**TCD**	**CEOU**	**CEOD**
1	X	X	X	X	X	0	0	1	0	CEOD
0	1	X	X	↑	Dn	Dn	TCU	TCD	CEOU	CEOD
0	1	X	X	↓	Dn	Dn	TCU	TCD	CEOU	CEOD
0	0	0	0	X	X	No Change	No Change	No Change	0	0
0	0	1	0	↑	X	Inc	TCU	TCD	CEOU	0
0	0	1	0	↓	X	Inc	TCU	TCD	CEOU	0
0	0	0	1	↑	X	Dec	TCU	TCD	0	CEOD
0	0	0	1	↓	X	Dec	TCU	TCD	0	CEOD
0	0	1	1	↑	X	Inc	TCU	TCD	Invalid	Invalid
0	0	1	1	↓	X	Inc	TCU	TCD	Invalid	Invalid
z = bit width - 1 TCU = Qz•Q(z-1)•Q(z-2)•...•Q0 TCD = Qz•Q(z-1)•Q(z-2)•...•Q0 CEOU = TCU•CEU CEOD = TCD•CED										

Design Entry Method

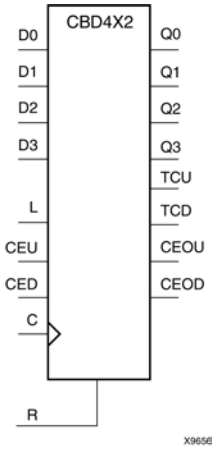
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CBD4X2

Macro: 4-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a synchronous, loadable, resettable, bidirectional dual edge triggered binary counter. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading.

The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, and clock enable outputs CEOU and CEOD go to Low and High, respectively, on the Low-to-High and High-to-Low clock (C) transition. The data on the D inputs loads into the counter on the Low-to-High and High-to-Low clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

All Q outputs increment when CEU is High, provided R and L are Low during the Low-to-High and High-to-Low clock transition. All Q outputs decrement when CED is High, provided R and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, the CEOU and CEOD outputs of each counter are, respectively, connected directly to the CEU and CED inputs of the next stage. The C, L, and R inputs are connected in parallel.

The maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs				
R	**L**	**CEU**	**CED**	**C**	**Dz : D0**	**Qz : Q0**	**TCU**	**TCD**	**CEOU**	**CEOD**
1	X	X	X	↑	X	0	0	1	0	CEOD
1	X	X	X	↓	X	0	0	1	0	CEOD
0	1	X	X	↑	Dn	Dn	TCU	TCD	CEOU	CEOD
0	1	X	X	↓	Dn	Dn	TCU	TCD	CEOU	CEOD
0	0	0	0	X	X	No Change	No Change	No Change	0	0
0	0	1	0	↑	X	Inc	TCU	TCD	CEOU	0
0	0	1	0	↓	X	Inc	TCU	TCD	CEOU	0
0	0	0	1	↑	X	Dec	TCU	TCD	0	CEOD
0	0	0	1	↓	X	Dec	TCU	TCD	0	CEOD
0	0	1	1	↑	X	Inc	TCU	TCD	Invalid	Invalid
0	0	1	1	↓	X	Inc	TCU	TCD	Invalid	Invalid

z = bit width - 1

TCU = Qz•Q(z-1)•Q(z-2)•...•Q0

TCD = Qz•Q(z-1)•Q(z-2)•...•Q0

CEOU = TCU•CEU

CEOD = TCD•CED

Design Entry Method

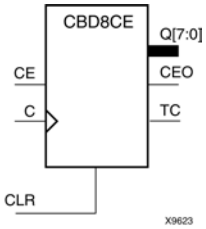
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CBD8CE

Macro: 8-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This element is an asynchronously clearable, cascadable dual edge triggered binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			Outputs		
CLR	**CE**	**C**	**Qz : Q0**	**TC**	**CEO**
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
0	1	↓	Inc	TC	CEO
z = bit width - 1					
TC = Qz•Q(z-1)•Q(z-2)•...•Q0					
CEO = TC•CE					

Design Entry Method

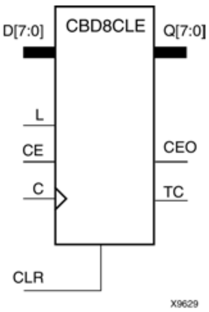
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CBD8CLE

Macro: 8-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This is a synchronously loadable, asynchronously clearable, cascadable dual edge triggered binary counters. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High and High-to-Low clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					Outputs		
CLR	**L**	**CE**	**C**	**Dz : D0**	**Qz : Q0**	**TC**	**CEO**
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	1	X	↓	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
0	0	1	↓	X	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE							

Design Entry Method

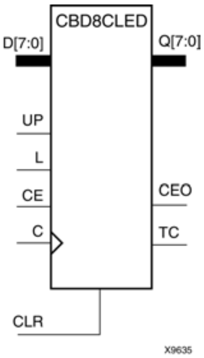
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CBD8CLED

Macro: 8-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional dual edge triggered binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High and High-to-Low clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

See CB2X1, CB4X1, CB8X1, CB16X1 for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs		
CLR	**L**	**CE**	**C**	**UP**	**Dz : D0**	**Qz : Q0**	**TC**	**CEO**
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	1	X	↓	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↓	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO
0	0	1	↓	0	X	Dec	TC	CEO
z = bit width - 1 TC = (QzQ(z-1)Q(z-2)...Q0UP) + (QzQ(z-1)Q(z-2)...Q0UP) CEO = TCCE								

Design Entry Method

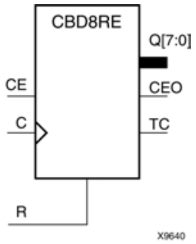
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CBD8RE

Macro: 8-Bit Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a synchronous, resettable, cascadable dual edge triggered binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero during the Low-to-High or High-to-Low clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n (t_{CE-TC}), where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			**Outputs**		
R	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	↑	0	0	0
1	X	↓	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
0	1	↓	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0) CEO = TC•CE					

Design Entry Method

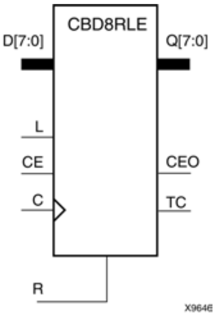
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CBD8RLE

Macro: 8-Bit Loadable Cascadable Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a synchronous, loadable, resettable, cascadable dual edge triggered binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) outputs to Low on the Low-to-High or High-to-Low clock (C) transition.

The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High and High-to-Low clock (C) transition, independent of the state of CE. The Q outputs increment when CE is High during the Low-to-High and High-to-Low clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High. The CEO output is High when all Q outputs and CE are High to allow direct cascading of counters.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					**Outputs**		
R	**L**	**CE**	**C**	**Dz : D0**	**Qz : Q0**	**TC**	**CEO**
1	X	X	↑	X	0	0	0
1	X	X	↓	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	1	X	↓	Dn	Dn	TC	CEO

Inputs					Outputs		
R	**L**	**CE**	**C**	**Dz : D0**	**Qz : Q0**	**TC**	**CEO**
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
0	0	1	↓	X	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE							

Design Entry Method

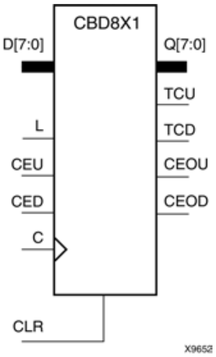
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CBD8X1

Macro: 8-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a synchronously loadable, asynchronously clearable, bidirectional dual edge triggered binary counters. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high speed cascading.

The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, clock enable outputs CEOU and CEOD go to Low and High, respectively, independent of clock transitions. The data on the D inputs loads into the counter on the Low-to-High and High-to-Low clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

The Q outputs increment when CEU is High, provided CLR and L are Low, during the Low-to-High and High-to-Low clock transition. The Q outputs decrement when CED is High, provided CLR and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, the CEOU and CEOD outputs of each counter are connected directly to the CEU and CED inputs, respectively, of the next stage. The clock, L, and CLR inputs are connected in parallel.

The maximum clocking frequency of these counters is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs				
CLR	L	CEU	CED	C	Dz–D0	Qz–Q0	TCU	TCD	CEOU	CEOD
1	X	X	X	X	X	0	0	1	0	CEOD
0	1	X	X	↑	Dn	Dn	TCU	TCD	CEOU	CEOD
0	1	X	X	↓	Dn	Dn	TCU	TCD	CEOU	CEOD
0	0	0	0	X	X	No Change	No Change	No Change	0	0
0	0	1	0	↑	X	Inc	TCU	TCD	CEOU	0
0	0	1	0	↓	X	Inc	TCU	TCD	CEOU	0
0	0	0	1	↑	X	Dec	TCU	TCD	0	CEOD
0	0	0	1	↓	X	Dec	TCU	TCD	0	CEOD
0	0	1	1	↑	X	Inc	TCU	TCD	Invalid	Invalid
0	0	1	1	↓	X	Inc	TCU	TCD	Invalid	Invalid
z = bit width - 1 TCU = Qz•Q(z-1)•Q(z-2)•...•Q0 TCD = Qz•Q(z-1)•Q(z-2)•...•Q0 CEOU = TCU•CEU CEOD = TCD•CED										

Design Entry Method

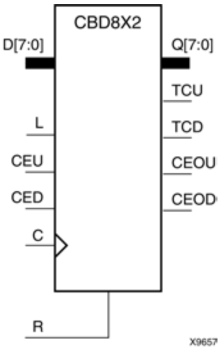
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CBD8X2

Macro: 8-Bit Loadable Cascadable Bidirectional Dual Edge Triggered Binary Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a synchronous, loadable, resettable, bidirectional dual edge triggered binary counter. It has separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading.

The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, and clock enable outputs CEOU and CEOD go to Low and High, respectively, on the Low-to-High and High-to-Low clock (C) transition. The data on the D inputs loads into the counter on the Low-to-High and High-to-Low clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

All Q outputs increment when CEU is High, provided R and L are Low during the Low-to-High and High-to-Low clock transition. All Q outputs decrement when CED is High, provided R and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, the CEOU and CEOD outputs of each counter are, respectively, connected directly to the CEU and CED inputs of the next stage. The C, L, and R inputs are connected in parallel.

The maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizable AND gates within the component. This results in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs				
R	**L**	**CEU**	**CED**	**C**	**Dz : D0**	**Qz : Q0**	**TCU**	**TCD**	**CEOU**	**CEOD**
1	X	X	X	↑	X	0	0	1	0	CEOD
1	X	X	X	↓	X	0	0	1	0	CEOD
0	1	X	X	↑	Dn	Dn	TCU	TCD	CEOU	CEOD
0	1	X	X	↓	Dn	Dn	TCU	TCD	CEOU	CEOD
0	0	0	0	X	X	No Change	No Change	No Change	0	0
0	0	1	0	↑	X	Inc	TCU	TCD	CEOU	0
0	0	1	0	↓	X	Inc	TCU	TCD	CEOU	0
0	0	0	1	↑	X	Dec	TCU	TCD	0	CEOD
0	0	0	1	↓	X	Dec	TCU	TCD	0	CEOD
0	0	1	1	↑	X	Inc	TCU	TCD	Invalid	Invalid
0	0	1	1	↓	X	Inc	TCU	TCD	Invalid	Invalid
z = bit width - 1 TCU = Qz•Q(z-1)•Q(z-2)•...•Q0 TCD = Qz•Q(z-1)•Q(z-2)•...•Q0 CEOU = TCU•CEU CEOD = TCD•CED										

Design Entry Method

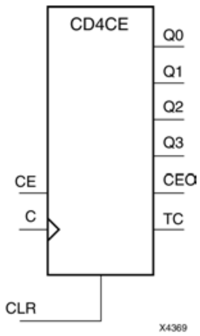
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CD4CE

Macro: 4-Bit Cascadable BCD Counter with Clock Enable and Asynchronous Clear



Supported Architectures

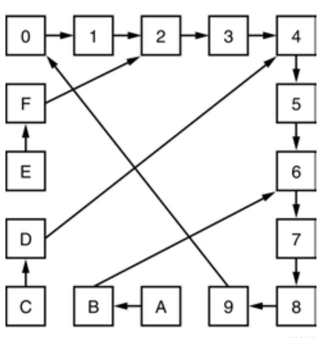
This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

CD4CE is a 4-bit (stage), asynchronous clearable, cascadable binary-coded-decimal (BCD) counter. The asynchronous clear input (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The Q outputs increment when clock enable (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:



Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			Outputs					
CLR	**CE**	**C**	**Q3**	**Q2**	**Q1**	**Q0**	**TC**	**CEO**
1	X	X	0	0	0	0	0	0
0	1	↑	Inc	Inc	Inc	Inc	TC	CEO
0	0	X	No Change	No Change	No Change	No Change	TC	0
0	1	X	1	0	0	1	1	1
TC = Q3•!Q2•!Q1•Q0 CEO = TC•CE								

Design Entry Method

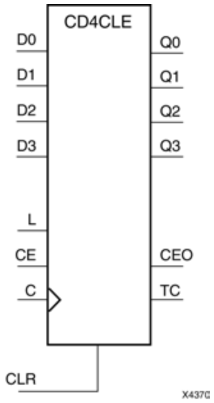
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CD4CLE

Macro: 4-Bit Loadable Cascadable BCD Counter with Clock Enable and Asynchronous Clear



Supported Architectures

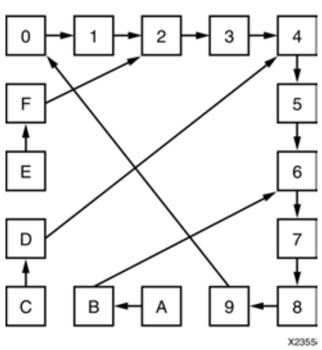
This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

CD4CLE is a 4-bit (stage), synchronously loadable, asynchronously clearable, binarycoded- decimal (BCD) counter. The asynchronous clear input (CLR) is the highest priority input. When (CLR) is High, all other inputs are ignored; the (Q) outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the (D) inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition. The (Q) outputs increment when clock enable input (CE) is High during the Low- to-High clock transition. The counter ignores clock transitions when (CE) is Low. The (TC) output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:



Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					Outputs					
CLR	**L**	**CE**	**D3 : D0**	**C**	**Q3**	**Q2**	**Q1**	**Q0**	**TC**	**CEO**
1	X	X	X	X	0	0	0	0	0	0
0	1	X	D3 : D0	↑	D3	D2	D1	D0	TC	CEO
0	0	1	X	↑	Inc	Inc	Inc	Inc	TC	CEO
0	0	0	X	X	No Change	No Change	No Change	No Change	TC	0
0	0	1	X	X	1	0	0	1	1	1
TC = Q3•!Q2•!Q1•Q0										
CEO = TC•CE										

Design Entry Method

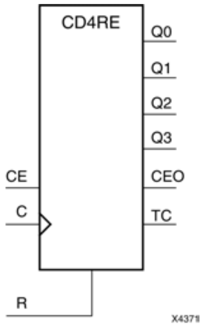
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CD4RE

Macro: 4-Bit Cascadable BCD Counter with Clock Enable and Synchronous Reset



Supported Architectures

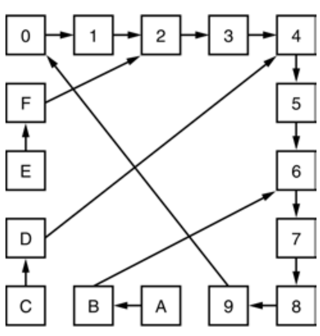
This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

CD4RE is a 4-bit (stage), synchronous resettable, cascadable binary-coded-decimal (BCD) counter. The synchronous reset input (R) is the highest priority input. When (R) is High, all other inputs are ignored; the (Q) outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High clock (C) transition. The (Q) outputs increment when the clock enable input (CE) is High during the Low-to- High clock transition. The counter ignores clock transitions when (CE) is Low. The (TC) output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:



Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n (t_{CE-TC}), where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			Outputs					
R	**CE**	**C**	**Q3**	**Q2**	**Q1**	**Q0**	**TC**	**CEO**
1	X	↑	0	0	0	0	0	0
0	1	↑	Inc	Inc	Inc	Inc	TC	CEO
0	0	X	No Change	No Change	No Change	No Change	TC	0
0	1	X	1	0	0	1	1	1
TC = Q3•!Q2•!Q1•Q0 CEO = TC•CE								

Design Entry Method

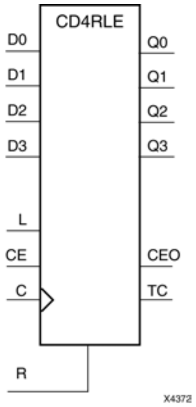
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CD4RLE

Macro: 4-Bit Loadable Cascadable BCD Counter with Clock Enable and Synchronous Reset



Supported Architectures

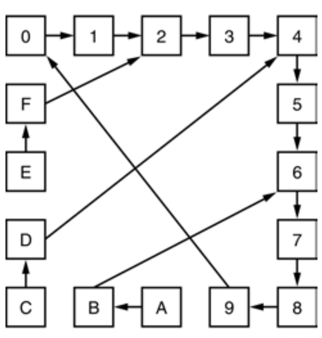
This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

CD4RLE is a 4-bit (stage), synchronous loadable, resettable, binary-coded-decimal (BCD) counter. The synchronous reset input (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:



Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n (t_{CE-TC}), where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					**Outputs**					
R	**L**	**CE**	**D3 : D0**	**C**	**Q3**	**Q2**	**Q1**	**Q0**	**TC**	**CEO**
1	X	X	X	↑	0	0	0	0	0	0
0	1	X	D3 : D0	↑	D3	D	D	D0	TC	CEO
0	0	1	X	↑	Inc	Inc	Inc	Inc	TC	CEO
0	0	0	X	X	No Change	No Change	No Change	No Change	TC	0
0	0	1	X	X	1	0	0	1	1	1
TC = Q3•!Q2•!Q1•Q0 CEO = TC•CE										

Design Entry Method

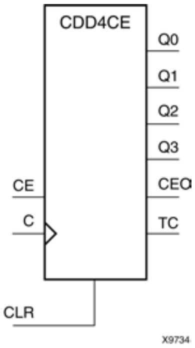
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CDD4CE

Macro: 4-Bit Cascadable Dual Edge Triggered BCD Counter with Clock Enable and Asynchronous Clear



Supported Architectures

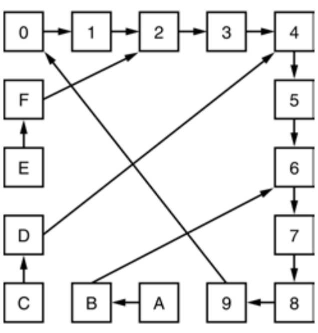
This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

CDD4CE is a 4-bit (stage), asynchronous clearable, cascadable dual edge triggered Binary-coded-decimal (BCD) counter. The asynchronous clear input (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The Q outputs increment when clock enable (CE) is High during the Low-to-High and High-to-Low clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low. The counter recovers to zero from any illegal state within the first clock cycle.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:



Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			Outputs					
CLR	**CE**	**C**	**Q3**	**Q2**	**Q1**	**Q0**	**TC**	**CEO**
1	X	X	0	0	0	0	0	0
0	1	↑	Inc	Inc	Inc	Inc	TC	CEO
0	1	↓	Inc	Inc	Inc	Inc	TC	CEO
0	0	X	No Change	No Change	No Change	No Change	TC	0
0	1	X	1	0	0	1	1	1
TC = Q3•!Q2•!Q1•Q0								

Design Entry Method

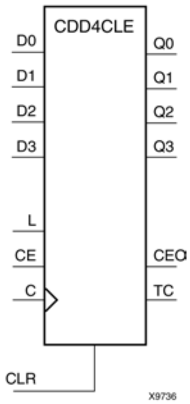
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CDD4CLE

Macro: 4-Bit Loadable Cascadable Dual Edge Triggered BCD Counter with Clock Enable and Asynchronous Clear



Supported Architectures

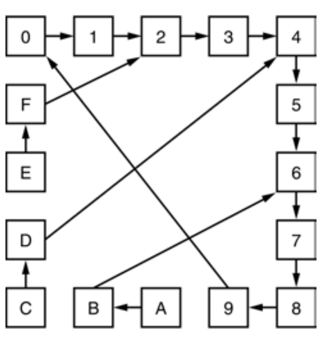
This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

CDD4CLE is a 4-bit (stage), synchronously loadable, asynchronously clearable, dual edge triggered Binary-coded-decimal (BCD) counter. The asynchronous clear input (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High and High-to-Low clock (C) transitions. The Q outputs increment when clock enable input (CE) is High during the Low- to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low. The counter recovers to zero from any illegal state within the first clock cycle.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:



Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					Outputs					
CLR	**L**	**CE**	**D3 : D0**	**C**	**Q3**	**Q2**	**Q1**	**Q0**	**TC**	**CEO**
1	X	X	X	X	0	0	0	0	0	0
0	1	X	D3 : D0	↑	D3	D2	D1	D0	TC	CEO
0	1	X	D3 : D0	↓	D3	D2	D1	D0	TC	CEO
0	0	1	X	↑	Inc	Inc	Inc	Inc	TC	CEO
0	0	1	X	↓	Inc	Inc	Inc	Inc	TC	CEO
0	0	0	X	X	No Change	No Change	No Change	No Change	TC	0
0	0	1	X	X	1	0	0	1	1	1
TC = Q3•!Q2•!Q1•Q0										
CEO = TC•CE										

Design Entry Method

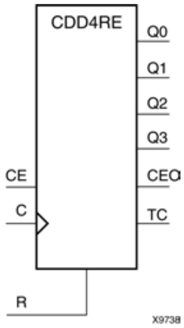
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CDD4RE

Macro: 4-Bit Cascadable Dual Edge Triggered BCD Counter with Clock Enable and Synchronous Reset



Supported Architectures

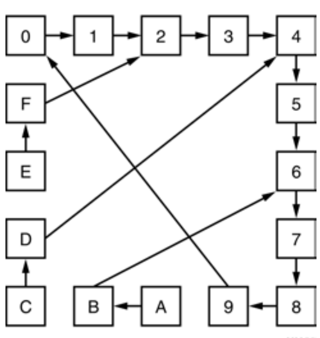
This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

CDD4RE is a 4-bit (stage), synchronous resettable, cascadable dual edge triggered binary-coded-decimal (BCD) counter. The synchronous reset input (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High or High-to-Low clock (C) transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low. The counter recovers to zero from any illegal state within the first clock cycle.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:



Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n (t_{CE-TC}), where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			Outputs					
R	**CE**	**C**	**Q3**	**Q2**	**Q1**	**Q0**	**TC**	**CEO**
1	X	↑	0	0	0	0	0	0
1	X	↓	0	0	0	0	0	0
0	1	↑	Inc	Inc	Inc	Inc	TC	CEO
0	1	↓	Inc	Inc	Inc	Inc	TC	CEO
0	0	X	No Change	No Change	No Change	No Change	TC	0
0	1	X	1	0	0	1	1	1
TC = Q3!Q2!Q1Q0 CEO = TCCE								

Design Entry Method

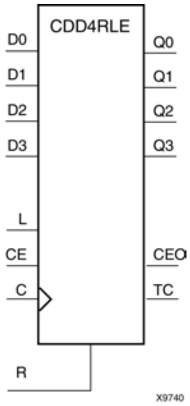
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CDD4RLE

Macro: 4-Bit Loadable Cascadable Dual Edge Triggered BCD Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This is a 4-bit (stage), synchronous loadable, resettable, dual edge triggered binary-coded-decimal (BCD) counter. The synchronous reset input (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High or High-to-Low clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High and High-to-Low clock (C) transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low. The counter recovers to zero from any illegal state within the first clock cycle.

Larger counters are created by connecting the count enable out (CEO) output of the first stage to the CE input of the next stage and connecting the R, L, and C inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n(tCE-TC), where n is the number of stages and the time tCE-TC is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Design Entry Method

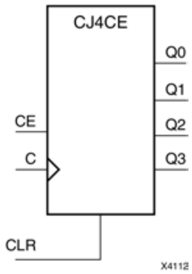
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CJ4CE

4-Bit Johnson Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a clearable Johnson/shift counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero, independent of clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2,and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when (CE) is Low.

The Q3 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied.

Logic Table

Inputs			Outputs	
CLR	**CE**	**C**	**Q0**	**Q1 through Q3**
1	X	X	0	0
0	0	X	No change	No change
0	1	↑	!q3	q0 through q2
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

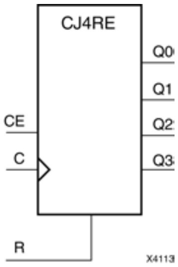
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CJ4RE

Macro: 4-Bit Johnson Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a resettable Johnson/shift counter. The synchronous reset (R) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero during the Low-to-High clock (C) transition. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when CE is Low.

The Q3 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied.

Logic Table

Inputs			Outputs	
R	**CE**	**C**	**Q0**	**Q1 through Q3**
1	X	↑	0	0
0	0	X	No change	No change
0	1	↑	!q3	q0 through q2
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

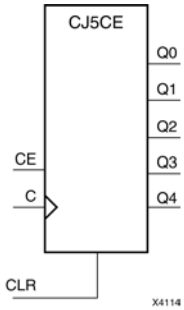
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CJ5CE

Macro: 5-Bit Johnson Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a clearable Johnson/shift counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero, independent of clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2,and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when (CE) is Low.

The Q4 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied.

Logic Table

Inputs			Outputs	
CLR	**CE**	**C**	**Q0**	**Q1 through Q4**
1	X	X	0	0
0	0	X	No change	No change
0	1	↑	!q4	q0 through q3
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

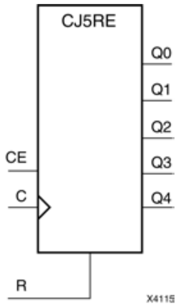
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CJ5RE

Macro: 5-Bit Johnson Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a resettable Johnson/shift counter. The synchronous reset (R) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero during the Low-to-High clock (C) transition. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when CE is Low.

The Q4 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied.

Logic Table

Inputs			Outputs	
R	**CE**	**C**	**Q0**	**Q1 through Q4**
1	X	↑	0	0
0	0	X	No change	No change
0	1	↑	!q4	q0 through q3
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

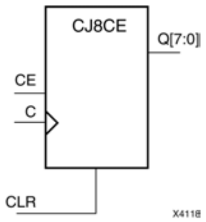
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CJ8CE

Macro: 8-Bit Johnson Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a clearable Johnson/shift counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero, independent of clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2,and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when (CE) is Low.

The Q7 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied.

Logic Table

Inputs			**Outputs**	
CLR	**CE**	**C**	**Q0**	**Q1 through Q8**
1	X	X	0	0
0	0	X	No change	No change
0	1	↑	!q7	q0 through q7
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

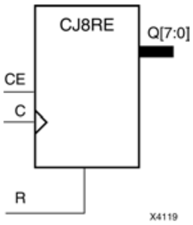
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CJ8RE

Macro: 8-Bit Johnson Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a resettable Johnson/shift counter. The synchronous reset (R) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero during the Low-to-High clock (C) transition. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when CE is Low.

The Q7 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied.

Logic Table

Inputs			Outputs	
R	**CE**	**C**	**Q0**	**Q1 through Q7**
1	X	↑	0	0
0	0	X	No change	No change
0	1	↑	!q7	q0 through q6
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

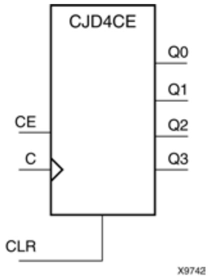
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CJD4CE

Macro: 4-Bit Dual Edge Triggered Johnson Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This element is a dual edge triggered clearable Johnson/shift counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and causes the data (Q) outputs to go to logic level zero independent of clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2,etc.) when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock transition. Clock transitions are ignored when CE is Low.

The Q3 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			Outputs	
CLR	**CE**	**C**	**Q0**	**Q1 through Q3**
1	X	X	0	0
0	0	X	No Change	No Change
0	1	↑	!q3	q0 through q2
0	1	↓	!q3	q0 through q2
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

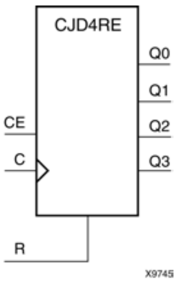
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CJD4RE

Macro: 4-Bit Dual Edge Triggered Johnson Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a resettable dual edge triggered Johnson/shift counter. The synchronous reset (R) input, when High, overrides all other inputs and causes the data (Q) outputs to go to logic level zero during the Low-to-High and High-to-Low clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2, etc.) when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock transition. Clock transitions are ignored when CE is Low.

The Q3 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			**Outputs**	
R	**CE**	**C**	**Q0**	**Q1 : Q3**
1	X	↑	0	0
1	X	↓	0	0
0	0	X	No Change	No Change
0	1	↑	!q3	q0 : q2
0	1	↓	!q3	q0 : q2
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

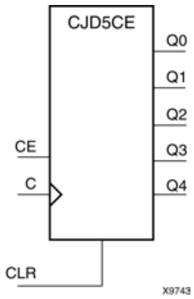
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CJD5CE

Macro: 5-Bit Dual Edge Triggered Johnson Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This element is a dual edge triggered clearable Johnson/shift counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and causes the data (Q) outputs to go to logic level zero independent of clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2,etc.) when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock transition. Clock transitions are ignored when CE is Low.

The Q4 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			Outputs	
CLR	**CE**	**C**	**Q0**	**Q1 through Q4**
1	X	X	0	0
0	0	X	No Change	No Change
0	1	↑	!q4	q0 through q3
0	1	↓	!q4	q0 through q3
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

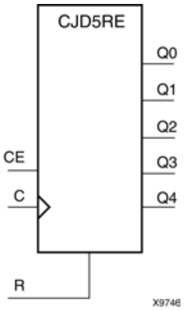
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CJD5RE

Macro: 5-Bit Dual Edge Triggered Johnson Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a resettable dual edge triggered Johnson/shift counter. The synchronous reset (R) input, when High, overrides all other inputs and causes the data (Q) outputs to go to logic level zero during the Low-to-High and High-to-Low clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2, etc.) when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock transition. Clock transitions are ignored when CE is Low.

The Q4 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			Outputs	
R	**CE**	**C**	**Q0**	**Q1 : Q4**
1	X	↑	0	0
1	X	↓	0	0
0	0	X	No Change	No Change
0	1	↑	!q4	q0 : q3
0	1	↓	!q4	q0 : q3
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

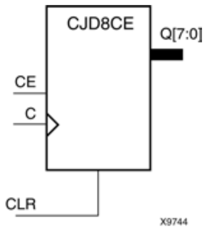
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CJD8CE

Macro: 8-Bit Dual Edge Triggered Johnson Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This element is a dual edge triggered clearable Johnson/shift counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and causes the data (Q) outputs to go to logic level zero independent of clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2,etc.) when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock transition. Clock transitions are ignored when CE is Low.

The Q7 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			Outputs	
CLR	**CE**	**C**	**Q0**	**Q1 through Q7**
1	X	X	0	0
0	0	X	No Change	No Change
0	1	↑	!q7	q0 through q6
0	1	↓	!q7	q0 through q6
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

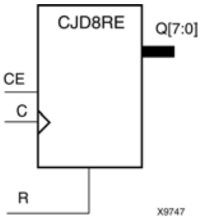
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CJD8RE

Macro: 8-Bit Dual Edge Triggered Johnson Counter with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a resettable dual edge triggered Johnson/shift counter. The synchronous reset (R) input, when High, overrides all other inputs and causes the data (Q) outputs to go to logic level zero during the Low-to-High and High-to-Low clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2, etc.) when the clock enable input (CE) is High during the Low-to-High and High-to-Low clock transition. Clock transitions are ignored when CE is Low.

The Q7 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			**Outputs**	
R	**CE**	**C**	**Q0**	**Q1 : Q7**
1	X	↑	0	0
1	X	↓	0	0
0	0	X	No Change	No Change
0	1	↑	!q7	q0 : q6
0	1	↓	!q7	q0 : q6
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

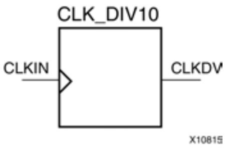
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV10

Primitive: Simple Global Clock Divide by 10



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 10.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32 or XC2C64. The CLKIN input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV10: Simple Clock Divide by 10
--            CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV10_inst : CLK_DIV10
port map (
   CLKDV => CLKDV,     -- Divided clock output
   CLKIN => CLKIN      -- Clock input
);

-- End of CLK_DIV10_inst instantiation
```

Verilog Instantiation Template

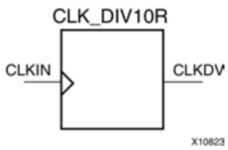
```
// CLK_DIV10: Simple Clock Divide by 10
//            CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV10 CLK_DIV10_inst (
   .CLKDV(CLKDV),    // Divided clock output
   .CLKIN(CLKIN)     // Clock input
);

// End of CLK_DIV10_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV10R

Primitive: Global Clock Divide by 10 with Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 10.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32 or XC2C64. The CLKIN and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV10R: Clock Divide by 10 with Synchronous Reset
--             CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV10R_inst : CLK_DIV10R
port map (
   CLKDV => CLKDV,     -- Divided clock output
   CDRST => CDRST,     -- Synchronous reset input
   CLKIN => CLKIN      -- Clock input
);

-- End of CLK_DIV10R_inst instantiation
```

Verilog Instantiation Template

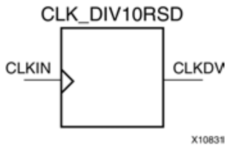
```
// CLK_DIV10R: Clock Divide by 10 with Synchronous Reset
//             CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV10R CLK_DIV10R_inst (
   .CLKDV(CLKDV),    // Divided clock output
   .CDRST(CDRST),    // Synchronous reset input
   .CLKIN(CLKIN)     // Clock input
);

// End of CLK_DIV10R_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV10RSD

Primitive: Global Clock Divide by 10 with Synchronous Reset and Start Delay



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 10.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32 or XC2C64. The CLKIN and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV10RSD: Clock Divide by 10 with Synchronous Reset and Start
-- Delay
--                CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV10RSD_inst : CLK_DIV10RSD
-- Edit the following generic to specify the number of clock cycles
-- to delay before starting.
generic map (
   DIVIDER_DELAY => 1)
port map (
   CLKDV => CLKDV,     -- Divided clock output
   CDRST => CDRST,     -- Synchronous reset input
   CLKIN => CLKIN      -- Clock input
);

-- End of CLK_DIV10RSD_inst instantiation
```

Verilog Instantiation Template

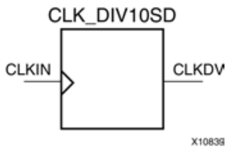
```
// CLK_DIV12RSD: Clock Divide by 12 with Synchronous Reset and Start
// Delay
//                CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV12RSD CLK_DIV12RSD_inst (
   .CLKDV(CLKDV), // Divided clock output
   .CDRST(CDRST), // Synchronous reset input
   .CLKIN(CLKIN)  // Clock input
);

// Edit the following defparam to specify the number of clock
// cycles to delay before starting. If the instance name to
// the clock divider is changed, that change needs to be
// reflected in the defparam statements.

defparam CLK_DIV12RSD_inst.DIVIDER_DELAY = 1;

// End of CLK_DIV12RSD_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV10SD

Primitive: Global Clock Divide by 10 with Start Delay



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 10.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32 or XC2C64. The CLKIN input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV10SD: Clock Divide by 10 with Start Delay
--              CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV10SD_inst : CLK_DIV10SD
-- Edit the following generic to specify the number of clock cycles
-- to delay before starting.
generic map (
   DIVIDER_DELAY => 1)
port map (
   CLKDV => CLKDV,    -- Divided clock output
   CLKIN => CLKIN     -- Clock input
);

-- End of CLK_DIV10SD_inst instantiation
```

Verilog Instantiation Template

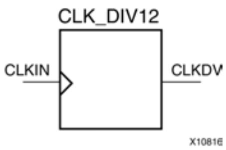
```
// CLK_DIV10SD: Clock Divide by 10 with Start Delay
//             CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV10SD CLK_DIV10SD_inst (
   .CLKDV(CLKDV), // Divided clock output
   .CDRST(CDRST), // Synchronous reset input
   .CLKIN(CLKIN)  // Clock input
);

// Edit the following defparam to specify the number of clock
// cycles to delay before starting. If the instance name to
// the clock divider is changed, that change needs to be
// reflected in the defparam statements.

defparam CLK_DIV10SD_inst.DIVIDER_DELAY = 1;

// End of CLK_DIV10SD_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV12

Primitive: Simple Global Clock Divide by 12



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 12.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32 or XC2C64. The CLKIN input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV12: Simple Clock Divide by 12
--            CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV12_inst : CLK_DIV12
port map (
   CLKDV => CLKDV,     -- Divided clock output
   CLKIN => CLKIN      -- Clock input
);

-- End of CLK_DIV12_inst instantiation
```

Verilog Instantiation Template

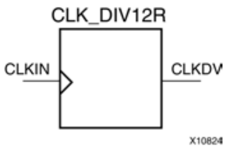
```
// CLK_DIV12: Simple Clock Divide by 12
//             CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV12 CLK_DIV12_inst (
   .CLKDV(CLKDV),    // Divided clock output
   .CLKIN(CLKIN)     // Clock input
);

// End of CLK_DIV12_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV12R

Primitive: Global Clock Divide by 12 with Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 12.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32 or XC2C64. The CLKIN and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV12R: Clock Divide by 12 with Synchronous Reset
--             CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV12R_inst : CLK_DIV12R
port map (
   CLKDV => CLKDV,    -- Divided clock output
   CDRST => CDRST,    -- Synchronous reset input
   CLKIN => CLKIN     -- Clock input
);

-- End of CLK_DIV12R_inst instantiation
```

Verilog Instantiation Template

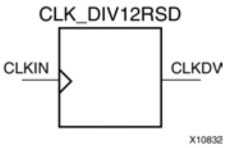
```
// CLK_DIV12R: Clock Divide by 12 with Synchronous Reset
//             CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV12R CLK_DIV12R_inst (
   .CLKDV(CLKDV),    // Divided clock output
   .CDRST(CDRST),    // Synchronous reset input
   .CLKIN(CLKIN)     // Clock input
);

// End of CLK_DIV12R_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV12RSD

Primitive: Global Clock Divide by 12 with Synchronous Reset and Start Delay



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 12.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32 or XC2C64. The CLKIN and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV12RSD: Clock Divide by 12 with Synchronous Reset and Start
-- Delay
--              CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV12RSD_inst : CLK_DIV12RSD
-- Edit the following generic to specify the number of clock cycles
-- to delay before starting.
generic map (
   DIVIDER_DELAY => 1)
port map (
   CLKDV => CLKDV,    -- Divided clock output
   CDRST => CDRST,    -- Synchronous reset input
   CLKIN => CLKIN     -- Clock input
);

-- End of CLK_DIV12RSD_inst instantiation
```

Verilog Instantiation Template

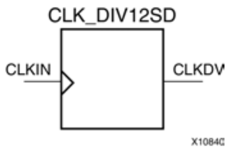
```
// CLK_DIV12RSD: Clock Divide by 12 with Synchronous Reset and Start
// Delay
//              CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV12RSD CLK_DIV12RSD_inst (
   .CLKDV(CLKDV), // Divided clock output
   .CDRST(CDRST), // Synchronous reset input
   .CLKIN(CLKIN)  // Clock input
);

// Edit the following defparam to specify the number of clock
// cycles to delay before starting. If the instance name to
// the clock divider is changed, that change needs to be
// reflected in the defparam statements.

defparam CLK_DIV12RSD_inst.DIVIDER_DELAY = 1;

// End of CLK_DIV12RSD_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV12SD

Primitive: Global Clock Divide by 12 with Start Delay



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 12.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32 or XC2C64. The CLKIN input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV12SD: Clock Divide by 12 with Start Delay
--              CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV12SD_inst : CLK_DIV12SD
-- Edit the following generic to specify the number of clock cycles
-- to delay before starting.
generic map (
   DIVIDER_DELAY => 1)
port map (
   CLKDV => CLKDV,    -- Divided clock output
   CLKIN => CLKIN     -- Clock input
);

-- End of CLK_DIV12SD_inst instantiation
```

Verilog Instantiation Template

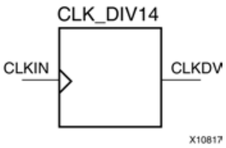
```
// CLK_DIV12SD: Clock Divide by 12 with Start Delay
//              CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV12SD CLK_DIV12SD_inst (
   .CLKDV(CLKDV), // Divided clock output
   .CDRST(CDRST), // Synchronous reset input
   .CLKIN(CLKIN)  // Clock input
);

// Edit the following defparam to specify the number of clock
// cycles to delay before starting. If the instance name to
// the clock divider is changed, that change needs to be
// reflected in the defparam statements.

defparam CLK_DIV12SD_inst.DIVIDER_DELAY = 1;

// End of CLK_DIV12SD_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV14

Primitive: Simple Global Clock Divide by 14



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 14.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32 or XC2C64. The CLKIN input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV14: Simple Clock Divide by 14
--            CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV14_inst : CLK_DIV14
port map (
   CLKDV => CLKDV,    -- Divided clock output
   CLKIN => CLKIN     -- Clock input
);

-- End of CLK_DIV14_inst instantiation
```

Verilog Instantiation Template

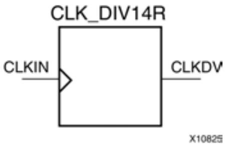
```
// CLK_DIV14: Simple Clock Divide by 14
//              CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV14 CLK_DIV14_inst (
   .CLKDV(CLKDV),    // Divided clock output
   .CLKIN(CLKIN)     // Clock input
);

// End of CLK_DIV14_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV14R

Primitive: Global Clock Divide by 14 with Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 14.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32 or XC2C64. The CLKIN and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV14R: Clock Divide by 14 with Synchronous Reset
--             CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV14R_inst : CLK_DIV14R
port map (
   CLKDV => CLKDV,     -- Divided clock output
   CDRST => CDRST,     -- Synchronous reset input
   CLKIN => CLKIN      -- Clock input
);

-- End of CLK_DIV14R_inst instantiation
```

Verilog Instantiation Template

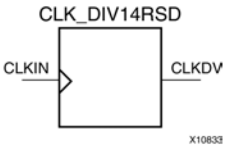
```
// CLK_DIV14R: Clock Divide by 14 with Synchronous Reset
//             CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV14R CLK_DIV14R_inst (
   .CLKDV(CLKDV),    // Divided clock output
   .CDRST(CDRST),    // Synchronous reset input
   .CLKIN(CLKIN)     // Clock input
);

// End of CLK_DIV14R_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV14RSD

Primitive: Global Clock Divide by 14 with Synchronous Reset and Start Delay



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 14.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32 or XC2C64. The CLKIN and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV14RSD: Clock Divide by 14 with Synchronous Reset and Start
-- Delay
--               CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV14RSD_inst : CLK_DIV14RSD
-- Edit the following generic to specify the number of clock cycles
-- to delay before starting.
generic map (
   DIVIDER_DELAY => 1)
port map (
   CLKDV => CLKDV,    -- Divided clock output
   CDRST => CDRST,    -- Synchronous reset input
   CLKIN => CLKIN     -- Clock input
);

-- End of CLK_DIV14RSD_inst instantiation
```

Verilog Instantiation Template

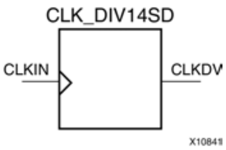
```
// CLK_DIV14RSD: Clock Divide by 14 with Synchronous Reset and Start
// Delay
//               CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV14RSD CLK_DIV14RSD_inst (
   .CLKDV(CLKDV), // Divided clock output
   .CDRST(CDRST), // Synchronous reset input
   .CLKIN(CLKIN)  // Clock input
);

// Edit the following defparam to specify the number of clock
// cycles to delay before starting. If the instance name to
// the clock divider is changed, that change needs to be
// reflected in the defparam statements.

defparam CLK_DIV14RSD_inst.DIVIDER_DELAY = 1;

// End of CLK_DIV14RSD_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV14SD

Primitive: Global Clock Divide by 14 with Start Delay



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 14.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32 or XC2C64. The CLKIN input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV14SD: Clock Divide by 14 with Start Delay
--              CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV14SD_inst : CLK_DIV14SD
-- Edit the following generic to specify the number of clock cycles
-- to delay before starting.
generic map (
   DIVIDER_DELAY => 1)
port map (
   CLKDV => CLKDV,    -- Divided clock output
   CLKIN => CLKIN     -- Clock input
);

-- End of CLK_DIV14SD_inst instantiation
```

Verilog Instantiation Template

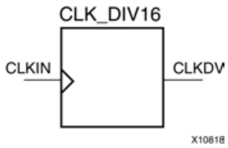
```
// CLK_DIV14SD: Clock Divide by 14 with Start Delay
//             CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV14SD CLK_DIV14SD_inst (
   .CLKDV(CLKDV), // Divided clock output
   .CDRST(CDRST), // Synchronous reset input
   .CLKIN(CLKIN)  // Clock input
);

// Edit the following defparam to specify the number of clock
// cycles to delay before starting. If the instance name to
// the clock divider is changed, that change needs to be
// reflected in the defparam statements.

defparam CLK_DIV14SD_inst.DIVIDER_DELAY = 1;

// End of CLK_DIV14SD_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV16

Primitive: Simple Global Clock Divide by 16



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 16.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32 or XC2C64. The CLKIN input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

When using this component, the dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV16: Simple Clock Divide by 16
--            CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV16_inst : CLK_DIV16
port map (
   CLKDV => CLKDV,    -- Divided clock output
   CLKIN => CLKIN     -- Clock input
);

-- End of CLK_DIV16_inst instantiation
```

Verilog Instantiation Template

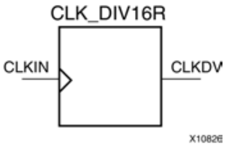
```
// CLK_DIV16: Simple Clock Divide by 16
//             CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV16 CLK_DIV16_inst (
   .CLKDV(CLKDV),    // Divided clock output
   .CLKIN(CLKIN)     // Clock input
);

// End of CLK_DIV16_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV16R

Primitive: Global Clock Divide by 16 with Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 16.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32 or XC2C64. The CLKIN and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV16R: Clock Divide by 16 with Synchronous Reset
--             CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV16R_inst : CLK_DIV16R
port map (
   CLKDV => CLKDV,     -- Divided clock output
   CDRST => CDRST,     -- Synchronous reset input
   CLKIN => CLKIN      -- Clock input
);

-- End of CLK_DIV16R_inst instantiation
```

Verilog Instantiation Template

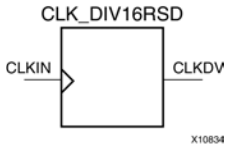
```
// CLK_DIV16R: Clock Divide by 16 with Synchronous Reset
//             CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV16R CLK_DIV16R_inst (
   .CLKDV(CLKDV),    // Divided clock output
   .CDRST(CDRST),    // Synchronous reset input
   .CLKIN(CLKIN)     // Clock input
);

// End of CLK_DIV16_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV16RSD

Primitive: Global Clock Divide by 16 with Synchronous Reset and Start Delay



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 16.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32 or XC2C64. The CLKIN and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV16RSD: Clock Divide by 16 with Synchronous Reset and Start
-- Delay
--                CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV16RSD_inst : CLK_DIV16RSD
-- Edit the following generic to specify the number of clock cycles
-- to delay before starting.
generic map (
   DIVIDER_DELAY => 1)
port map (
   CLKDV => CLKDV,     -- Divided clock output
   CDRST => CDRST,     -- Synchronous reset input
   CLKIN => CLKIN      -- Clock input
);

-- End of CLK_DIV16RSD_inst instantiation
```

Verilog Instantiation Template

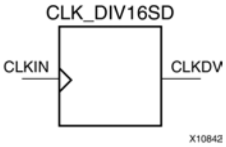
```
// CLK_DIV16RSD: Clock Divide by 16 with Synchronous Reset and Start
// Delay
//                CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV16RSD CLK_DIV16RSD_inst (
   .CLKDV(CLKDV), // Divided clock output
   .CDRST(CDRST), // Synchronous reset input
   .CLKIN(CLKIN)  // Clock input
);

// Edit the following defparam to specify the number of clock
// cycles to delay before starting. If the instance name to
// the clock divider is changed, that change needs to be
// reflected in the defparam statements.

defparam CLK_DIV16RSD_inst.DIVIDER_DELAY = 1;

// End of CLK_DIV16RSD_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV16SD

Primitive: Global Clock Divide by 16 with Start Delay



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 16.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32 or XC2C64. The CLKIN input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV16SD: Clock Divide by 16 with Start Delay
--              CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV16SD_inst : CLK_DIV16SD
-- Edit the following generic to specify the number of clock cycles
-- to delay before starting.
generic map (
   DIVIDER_DELAY => 1)
port map (
   CLKDV => CLKDV,    -- Divided clock output
   CLKIN => CLKIN     -- Clock input
);

-- End of CLK_DIV16SD_inst instantiation
```

Verilog Instantiation Template

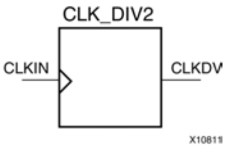
```
// CLK_DIV16SD: Clock Divide by 16 with Start Delay
//              CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV16SD CLK_DIV16SD_inst (
   .CLKDV(CLKDV), // Divided clock output
   .CDRST(CDRST), // Synchronous reset input
   .CLKIN(CLKIN)  // Clock input
);

// Edit the following defparam to specify the number of clock
// cycles to delay before starting. If the instance name to
// the clock divider is changed, that change needs to be
// reflected in the defparam statements.

defparam CLK_DIV16SD_inst.DIVIDER_DELAY = 1;

// End of CLK_DIV16SD_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV2

Primitive: Simple Global Clock Divide by 2



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 2.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32 or XC2C64. The CLKIN input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV2: Simple Clock Divide by 2
--             CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV2_inst : CLK_DIV2
port map (
   CLKDV => CLKDV,     -- Divided clock output
   CLKIN => CLKIN      -- Clock input
);

-- End of CLK_DIV2_inst instantiation
```

Verilog Instantiation Template

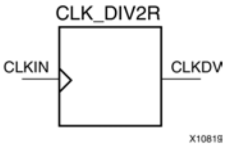
```
// CLK_DIV2: Simple Clock Divide by 2
//            CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV2 CLK_DIV2_inst (
   .CLKDV(CLKDV),    // Divided clock output
   .CLKIN(CLKIN)     // Clock input
);

// End of CLK_DIV2_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV2R

Primitive: Global Clock Divide by 2 with Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 2.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32 or XC2C64. The CLKIN and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV2R: Clock Divide by 2 with Synchronous Reset
--               CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV2R_inst : CLK_DIV2R
port map (
   CLKDV => CLKDV,     -- Divided clock output
   CDRST => CDRST,     -- Synchronous reset input
   CLKIN => CLKIN      -- Clock input
);

-- End of CLK_DIV2R_inst instantiation
```

Verilog Instantiation Template

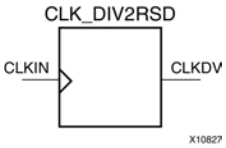
```
// CLK_DIV2R: Clock Divide by 2 with Synchronous Reset
//            CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV2R CLK_DIV2R_inst (
   .CLKDV(CLKDV),    // Divided clock output
   .CDRST(CDRST),    // Synchronous reset input
   .CLKIN(CLKIN)     // Clock input
);

// End of CLK_DIV2R_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV2RSD

Primitive: Global Clock Divide by 2 with Synchronous Reset and Start Delay



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 2.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32 or XC2C64. The CLKIN and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV2RSD: Clock Divide by 2 with Synchronous Reset and Start
-- Delay
--               CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV2RSD_inst : CLK_DIV2RSD
-- Edit the following generic to specify the number of clock cycles
-- to delay before starting.
generic map (
   DIVIDER_DELAY => 1)
port map (
   CLKDV => CLKDV,     -- Divided clock output
   CDRST => CDRST,     -- Synchronous reset input
   CLKIN => CLKIN      -- Clock input
);

-- End of CLK_DIV2RSD_inst instantiation
```

Verilog Instantiation Template

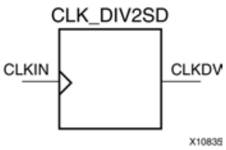
```
// CLK_DIV2RSD: Clock Divide by 2 with Synchronous Reset and Start
// Delay
//               CoolRunner-II
// Xilinx HDL Language Template, version 10.1

   CLK_DIV2RSD CLK_DIV2RSD_inst (
      .CLKDV(CLKDV), // Divided clock output
      .CDRST(CDRST), // Synchronous reset input
      .CLKIN(CLKIN)  // Clock input
   );

// Edit the following defparam to specify the number of clock
// cycles to delay before starting. If the instance name to
// the clock divider is changed, that change needs to be
// reflected in the defparam statements.

   defparam CLK_DIV2RSD_inst.DIVIDER_DELAY = 1;

// End of CLK_DIV2RSD_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV2SD

Primitive: Global Clock Divide by 2 with Start Delay



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 2.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32 or XC2C64. The CLKIN input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV2SD: Clock Divide by 2 with Start Delay
--             CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV2SD_inst : CLK_DIV2SD
-- Edit the following generic to specify the number of clock cycles
-- to delay before starting.
generic map (
   DIVIDER_DELAY => 1)
port map (
   CLKDV => CLKDV,    -- Divided clock output
   CLKIN => CLKIN     -- Clock input
);

-- End of CLK_DIV2SD_inst instantiation
```

Verilog Instantiation Template

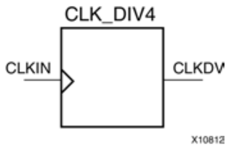
```
// CLK_DIV2SD: Clock Divide by 2 with Start Delay
//             CoolRunner-II
// Xilinx HDL Language Template, version 10.1

   CLK_DIV2SD CLK_DIV2SD_inst (
      .CLKDV(CLKDV), // Divided clock output
      .CDRST(CDRST), // Synchronous reset input
      .CLKIN(CLKIN)  // Clock input
   );

// Edit the following defparam to specify the number of clock
// cycles to delay before starting. If the instance name to
// the clock divider is changed, that change needs to be
// reflected in the defparam statements.

   defparam CLK_DIV2SD_inst.DIVIDER_DELAY = 1;

// End of CLK_DIV2SD_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV4

Primitive: Simple Global Clock Divide by 4



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 4.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32 or XC2C64. The CLKIN input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV4: Simple Clock Divide by 4
--             CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV4_inst : CLK_DIV4
port map (
   CLKDV => CLKDV,     -- Divided clock output
   CLKIN => CLKIN      -- Clock input
);

-- End of CLK_DIV4_inst instantiation
```

Verilog Instantiation Template

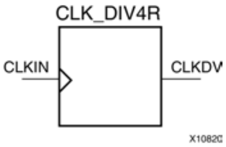
```
// CLK_DIV4: Simple Clock Divide by 4
//             CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV4 CLK_DIV4_inst (
   .CLKDV(CLKDV),    // Divided clock output
   .CLKIN(CLKIN)     // Clock input
);

// End of CLK_DIV4_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV4R

Primitive: Global Clock Divide by 4 with Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 4.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32 or XC2C64. The CLKIN and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV4R: Clock Divide by 4 with Synchronous Reset
--            CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV4R_inst : CLK_DIV4R
port map (
   CLKDV => CLKDV,    -- Divided clock output
   CDRST => CDRST,    -- Synchronous reset input
   CLKIN => CLKIN     -- Clock input
);

-- End of CLK_DIV4R_inst instantiation
```

Verilog Instantiation Template

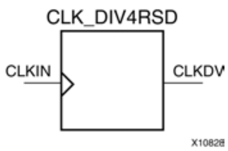
```
// CLK_DIV4R: Clock Divide by 4 with Synchronous Reset
//            CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV4R CLK_DIV4R_inst (
   .CLKDV(CLKDV),    // Divided clock output
   .CDRST(CDRST),    // Synchronous reset input
   .CLKIN(CLKIN)     // Clock input
);

// End of CLK_DIV4R_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV4RSD

Primitive: Global Clock Divide by 4 with Synchronous Reset and Start Delay



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 4.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32 or XC2C64. The CLKIN and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV4RSD: Clock Divide by 4 with Synchronous Reset and Start
-- Delay
--               CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

   CLK_DIV4RSD_inst : CLK_DIV4RSD
-- Edit the following generic to specify the number of clock cycles
-- to delay before starting.
generic map (
   DIVIDER_DELAY => 1)
port map (
   CLKDV => CLKDV,     -- Divided clock output
   CDRST => CDRST,     -- Synchronous reset input
   CLKIN => CLKIN      -- Clock input
);

-- End of CLK_DIV4RSD_inst instantiation
```

Verilog Instantiation Template

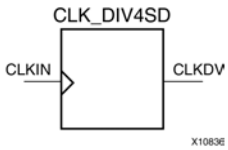
```
// CLK_DIV4RSD: Clock Divide by 4 with Synchronous Reset and Start
// Delay
//               CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV4RSD CLK_DIV4RSD_inst (
   .CLKDV(CLKDV), // Divided clock output
   .CDRST(CDRST), // Synchronous reset input
   .CLKIN(CLKIN)  // Clock input
);

// Edit the following defparam to specify the number of clock
// cycles to delay before starting. If the instance name to
// the clock divider is changed, that change needs to be
// reflected in the defparam statements.

defparam CLK_DIV4RSD_inst.DIVIDER_DELAY = 1;

// End of CLK_DIV4RSD_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV4SD

Primitive: Global Clock Divide by 4 with Start Delay



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 4.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32 or XC2C64. The CLKIN input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV4SD: Clock Divide by 4 with Start Delay
--             CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV4SD_inst : CLK_DIV4SD
-- Edit the following generic to specify the number of clock cycles
-- to delay before starting.
generic map (
   DIVIDER_DELAY => 1)
port map (
   CLKDV => CLKDV,    -- Divided clock output
   CLKIN => CLKIN     -- Clock input
);

-- End of CLK_DIV4SD_inst instantiation
```

Verilog Instantiation Template

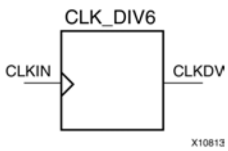
```
// CLK_DIV4SD: Clock Divide by 4 with Start Delay
//             CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV4SD CLK_DIV4SD_inst (
   .CLKDV(CLKDV), // Divided clock output
   .CDRST(CDRST), // Synchronous reset input
   .CLKIN(CLKIN)  // Clock input
);

// Edit the following defparam to specify the number of clock
// cycles to delay before starting. If the instance name to
// the clock divider is changed, that change needs to be
// reflected in the defparam statements.

defparam CLK_DIV4SD_inst.DIVIDER_DELAY = 1;

// End of CLK_DIV4SD_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV6

Primitive: Simple Global Clock Divide by 6



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 6.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32 or XC2C64. The CLKIN input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV6: Simple Clock Divide by 6
--             CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV6_inst : CLK_DIV6
port map (
   CLKDV => CLKDV,     -- Divided clock output
   CLKIN => CLKIN      -- Clock input
);

-- End of CLK_DIV6_inst instantiation
```

Verilog Instantiation Template

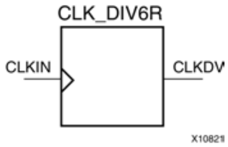
```
// CLK_DIV6: Simple Clock Divide by 6
//            CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV6 CLK_DIV6_inst (
   .CLKDV(CLKDV),    // Divided clock output
   .CLKIN(CLKIN)     // Clock input
);

// End of CLK_DIV6_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV6R

Primitive: Global Clock Divide by 6 with Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 6.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32 or XC2C64. The CLKIN and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV6R: Clock Divide by 6 with Synchronous Reset
--            CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV6R_inst : CLK_DIV6R
port map (
   CLKDV => CLKDV,     -- Divided clock output
   CDRST => CDRST,     -- Synchronous reset input
   CLKIN => CLKIN      -- Clock input
);

-- End of CLK_DIV6R_inst instantiation
```

Verilog Instantiation Template

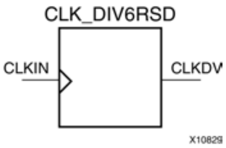
```
// CLK_DIV6R: Clock Divide by 6 with Synchronous Reset
//             CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV6R CLK_DIV6R_inst (
   .CLKDV(CLKDV),    // Divided clock output
   .CDRST(CDRST),    // Synchronous reset input
   .CLKIN(CLKIN)     // Clock input
);

// End of CLK_DIV6R_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV6RSD

Primitive: Global Clock Divide by 6 with Synchronous Reset and Start Delay



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 6.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32 or XC2C64. The CLKIN and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV6RSD: Clock Divide by 6 with Synchronous Reset and Start
-- Delay
--               CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV6RSD_inst : CLK_DIV6RSD
-- Edit the following generic to specify the number of clock cycles
-- to delay before starting.
generic map (
   DIVIDER_DELAY => 1)
port map (
   CLKDV => CLKDV,    -- Divided clock output
   CDRST => CDRST,    -- Synchronous reset input
   CLKIN => CLKIN     -- Clock input
);

-- End of CLK_DIV6RSD_inst instantiation
```

Verilog Instantiation Template

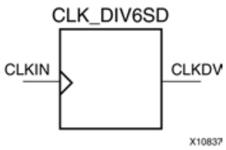
```
// CLK_DIV6RSD: Clock Divide by 6 with Synchronous Reset and Start
// Delay
//               CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV6RSD CLK_DIV6RSD_inst (
   .CLKDV(CLKDV), // Divided clock output
   .CDRST(CDRST), // Synchronous reset input
   .CLKIN(CLKIN)  // Clock input
);

// Edit the following defparam to specify the number of clock
// cycles to delay before starting. If the instance name to
// the clock divider is changed, that change needs to be
// reflected in the defparam statements.

defparam CLK_DIV6RSD_inst.DIVIDER_DELAY = 1;

// End of CLK_DIV6RSD_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV6SD

Primitive: Global Clock Divide by 6 with Start Delay



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

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The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

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This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV6SD: Clock Divide by 6 with Start Delay
--             CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV6SD_inst : CLK_DIV6SD
-- Edit the following generic to specify the number of clock cycles
-- to delay before starting.
generic map (
   DIVIDER_DELAY => 1)
port map (
   CLKDV => CLKDV,    -- Divided clock output
   CLKIN => CLKIN     -- Clock input
);

-- End of CLK_DIV4SD_inst instantiation
```

Verilog Instantiation Template

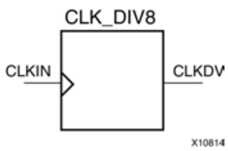
```
// CLK_DIV6SD: Clock Divide by 6 with Start Delay
//             CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV6SD CLK_DIV6SD_inst (
   .CLKDV(CLKDV), // Divided clock output
   .CDRST(CDRST), // Synchronous reset input
   .CLKIN(CLKIN)  // Clock input
);

// Edit the following defparam to specify the number of clock
// cycles to delay before starting. If the instance name to
// the clock divider is changed, that change needs to be
// reflected in the defparam statements.

defparam CLK_DIV6SD_inst.DIVIDER_DELAY = 1;

// End of CLK_DIV6SD_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV8

Primitive: Simple Global Clock Divide by 8



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 8.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32 or XC2C64. The CLKIN input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV8: Simple Clock Divide by 8
--             CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV8_inst : CLK_DIV8
port map (
   CLKDV => CLKDV,     -- Divided clock output
   CLKIN => CLKIN      -- Clock input
);

-- End of CLK_DIV8_inst instantiation
```

Verilog Instantiation Template

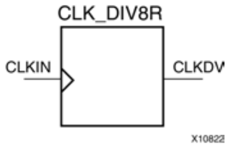
```
// CLK_DIV8: Simple Clock Divide by 8
//            CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV8 CLK_DIV8_inst (
   .CLKDV(CLKDV),    // Divided clock output
   .CLKIN(CLKIN)     // Clock input
);

// End of CLK_DIV8_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV8R

Primitive: Global Clock Divide by 8 with Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 8.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32 or XC2C64. The CLKIN and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV8R: Clock Divide by 8 with Synchronous Reset
--            CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV8R_inst : CLK_DIV8R
port map (
   CLKDV => CLKDV,    -- Divided clock output
   CDRST => CDRST,    -- Synchronous reset input
   CLKIN => CLKIN     -- Clock input
);

-- End of CLK_DIV8R_inst instantiation
```

Verilog Instantiation Template

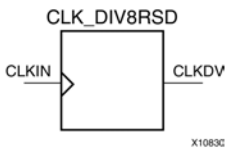
```
// CLK_DIV8R: Clock Divide by 8 with Synchronous Reset
//            CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV8R CLK_DIV8R_inst (
   .CLKDV(CLKDV),    // Divided clock output
   .CDRST(CDRST),    // Synchronous reset input
   .CLKIN(CLKIN)     // Clock input
);

// End of CLK_DIV8R_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV8RSD

Primitive: Global Clock Divide by 8 with Synchronous Reset and Start Delay



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 8.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner™-II devices, but not the XC2C32 or XC2C64. The CLKIN and CDRST inputs can only be connected to the device gclk<2> and CDRST pins. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The CDRST input is an active High synchronous reset. If CDRST is input High when the CLKDV output is High, the CLKDV output remains High to complete the last clock pulse, and then goes Low.

The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved for the sole purpose of a reset for the clock divider and may not be utilized for other user logic even if the reset port is unused.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV8RSD: Clock Divide by 8 with Synchronous Reset and Start
-- Delay
--               CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV8RSD_inst : CLK_DIV8RSD
-- Edit the following generic to specify the number of clock cycles
-- to delay before starting.
generic map (
   DIVIDER_DELAY => 1)
port map (
   CLKDV => CLKDV,    -- Divided clock output
   CDRST => CDRST,    -- Synchronous reset input
   CLKIN => CLKIN     -- Clock input
);

-- End of CLK_DIV8RSD_inst instantiation
```

Verilog Instantiation Template

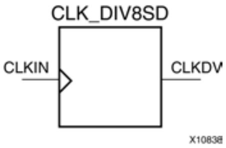
```
// CLK_DIV8RSD: Clock Divide by 8 with Synchronous Reset and Start
// Delay
//               CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV8RSD CLK_DIV8RSD_inst (
   .CLKDV(CLKDV), // Divided clock output
   .CDRST(CDRST), // Synchronous reset input
   .CLKIN(CLKIN)  // Clock input
);

// Edit the following defparam to specify the number of clock
// cycles to delay before starting. If the instance name to
// the clock divider is changed, that change needs to be
// reflected in the defparam statements.

defparam CLK_DIV8RSD_inst.DIVIDER_DELAY = 1;

// End of CLK_DIV8RSD_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CLK_DIV8SD

Primitive: Global Clock Divide by 8 with Start Delay



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element divides a user-provided external clock signal gclk<2> by 8.

Only one clock divider may be used per design. The global clock divider is available on the XC2C128, XC2C256, XC2C384, and XC2C512 CoolRunner-II devices, but not the XC2C32 or XC2C64. The CLKIN input can only be connected to the device gclk<2> pin. The duty cycle of the CLKDV output is 50-50. The CLKDV output can only connect to clock inputs of synchronous elements. It cannot be used as combinatorial logic, and should not be routed directly to an output pin.

The start delay function delays the start of the CLKDV output by (n + 1) clocks, where n is the divisor for the clock divider.

The CLKDV output is reset low by power-on reset circuitry.

The dedicated clock divider reset pin on the device is reserved and may not be used by user logic.

Design Entry Method

This design element can be used in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- CLK_DIV8SD: Clock Divide by 8 with Start Delay
--            CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

CLK_DIV8SD_inst : CLK_DIV8SD
-- Edit the following generic to specify the number of clock cycles
-- to delay before starting.
generic map (
   DIVIDER_DELAY => 1)
port map (
   CLKDV => CLKDV,    -- Divided clock output
   CLKIN => CLKIN     -- Clock input
);

-- End of CLK_DIV8SD_inst instantiation
```

Verilog Instantiation Template

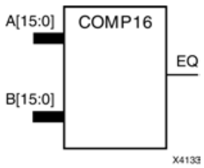
```
// CLK_DIV8SD: Clock Divide by 8 with Start Delay
//             CoolRunner-II
// Xilinx HDL Language Template, version 10.1

CLK_DIV8SD CLK_DIV8SD_inst (
   .CLKDV(CLKDV), // Divided clock output
   .CDRST(CDRST), // Synchronous reset input
   .CLKIN(CLKIN)  // Clock input
);

// Edit the following defparam to specify the number of clock
// cycles to delay before starting. If the instance name to
// the clock divider is changed, that change needs to be
// reflected in the defparam statements.

defparam CLK_DIV8SD_inst.DIVIDER_DELAY = 1;

// End of CLK_DIV8SD_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

COMP16

Macro: 16-Bit Identity Comparator



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 16-bit identity comparator. The equal output (EQ) is high when A15 : A0 and B15 : B0 are equal.

Equality is determined by a bit comparison of the two words. When any two of the corresponding bits from each word are not the same, the EQ output is Low.

Design Entry Method

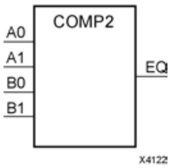
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

COMP2

Macro: 2-Bit Identity Comparator



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 2-bit identity comparator. The equal output (EQ) is High when the two words A1 : A0 and B1 : B0 are equal.

Equality is determined by a bit comparison of the two words. When any two of the corresponding bits from each word are not the same, the EQ output is Low.

Design Entry Method

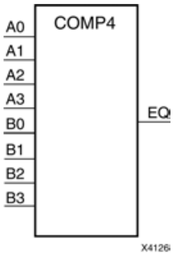
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

COMP4

Macro: 4-Bit Identity Comparator



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 4-bit identity comparator. The equal output (EQ) is high when A3 : A0 and B3 : B0 are equal.

Equality is determined by a bit comparison of the two words. When any two of the corresponding bits from each word are not the same, the EQ output is Low.

Design Entry Method

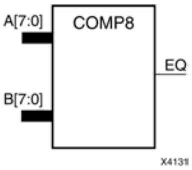
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

COMP8

Macro: 8-Bit Identity Comparator



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is an 8-bit identity comparator. The equal output (EQ) is high when A7 : A0 and B7 : B0 are equal.

Equality is determined by a bit comparison of the two words. When any two of the corresponding bits from each word are not the same, the EQ output is Low.

Design Entry Method

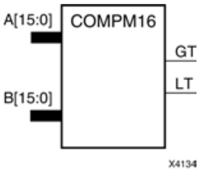
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

COMPM16

Macro: 16-Bit Magnitude Comparator



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 16-bit magnitude comparator that compare two positive Binary-weighted words. It compares A15 : A0 and B15 : B0, where A15 and B15 are the most significant bits.

The greater-than output (GT) is High when A > B, and the less-than output (LT) is High when A < B When the two words are equal, both GT and LT are Low. Equality can be measured with this macro by comparing both outputs with a NOR gate.

Logic Table

Inputs								Outputs	
A7, B7	**A6, B6**	**A5, B5**	**A4, B4**	**A3, B3**	**A2, B2**	**A1, B1**	**A0, B0**	**GT**	**LT**
A7>B7	X	X	X	X	X	X	X	1	0
A7<B7	X	X	X	X	X	X	X	0	1
A7=B7	A6>B6	X	X	X	X	X	X	1	0
A7=B7	A6<B6	X	X	X	X	X	X	0	1
A7=B7	A6=B6	A5>B5	X	X	X	X	X	1	0
A7=B7	A6=B6	A5<B5	X	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4>B4	X	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4<B4	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3>B3	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3<B3	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2>B2	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2<B2	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1>B1	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1<B1	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0>B0	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0<B0	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0=B0	0	0

Design Entry Method

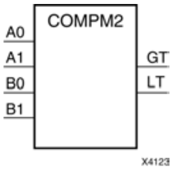
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

COMPM2

Macro: 2-Bit Magnitude Comparator



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 2-bit magnitude comparator that compare two positive binary-weighted words. It compares A1 : A0 and B1 : B0, where A1 and B1 are the most significant bits.

The greater-than output (GT) is High when A > B, and the less-than output (LT) is High when A < B When the two words are equal, both GT and LT are Low. Equality can be measured with this macro by comparing both outputs with a NOR gate.

Logic Table

Inputs				**Outputs**	
A1	**B1**	**A0**	**B0**	**GT**	**LT**
0	0	0	0	0	0
0	0	1	0	1	0
0	0	0	1	0	1
0	0	1	1	0	0
1	1	0	0	0	0
1	1	1	0	1	0
1	1	0	1	0	1
1	1	1	1	0	0
1	0	X	X	1	0
0	1	X	X	0	1

Design Entry Method

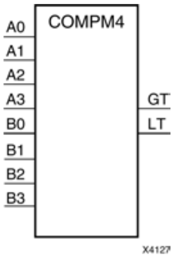
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

COMPM4

Macro: 4-Bit Magnitude Comparator



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 4-bit magnitude comparator that compare two positive Binary-weighted words. It compares A3 : A0 and B3 : B0, where A3 and B3 are the most significant bits.

The greater-than output (GT) is High when A > B, and the less-than output (LT) is High when A < B When the two words are equal, both GT and LT are Low. Equality can be measured with this macro by comparing both outputs with a NOR gate.

Logic Table

Inputs				Outputs	
A3, B3	**A2, B2**	**A1, B1**	**A0, B0**	**GT**	**LT**
A3>B3	X	X	X	1	0
A3<B3	X	X	X	0	1
A3=B3	A2>B2	X	X	1	0
A3=B3	A2<B2	X	X	0	1
A3=B3	A2=B2	A1>B1	X	1	0
A3=B3	A2=B2	A1<B1	X	0	1
A3=B3	A2=A2	A1=B1	A0>B0	1	0
A3=B3	A2=B2	A1=B1	A0<B0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	0

Design Entry Method

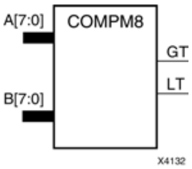
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

COMPM8

Macro: 8-Bit Magnitude Comparator



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is an 8-bit magnitude comparator that compare two positive Binary-weighted words. It compares A7 : A0 and B7 : B0, where A7 and B7 are the most significant bits.

The greater-than output (GT) is High when A > B, and the less-than output (LT) is High when A < B When the two words are equal, both GT and LT are Low. Equality can be measured with this macro by comparing both outputs with a NOR gate.

Logic Table

Inputs								Outputs	
A7, B7	**A6, B6**	**A5, B5**	**A4, B4**	**A3, B3**	**A2, B2**	**A1, B1**	**A0, B0**	**GT**	**LT**
A7>B7	X	X	X	X	X	X	X	1	0
A7<B7	X	X	X	X	X	X	X	0	1
A7=B7	A6>B6	X	X	X	X	X	X	1	0
A7=B7	A6<B6	X	X	X	X	X	X	0	1
A7=B7	A6=B6	A5>B5	X	X	X	X	X	1	0
A7=B7	A6=B6	A5<B5	X	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4>B4	X	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4<B4	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3>B3	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3<B3	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2>B2	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2<B2	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1>B1	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1<B1	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0>B0	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0<B0	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0=B0	0	0

Design Entry Method

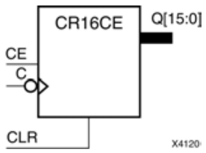
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CR16CE

Macro: 16-Bit Negative-Edge Binary Ripple Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 16-bit cascadable, clearable, binary ripple counter with clock enable and asynchronous clear.

Larger counters can be created by connecting the last Q output of the first stage to the clock input of the next stage. CLR and CE inputs are connected in parallel. The clock period is not affected by the overall length of a ripple counter. The overall clock-to-output propagation is n(t_{C-Q}), where n is the number of stages and the time t_{C-Q} is the C-to-Qz propagation delay of each stage.

This counter is asynchronously cleared, outputs Low, when power is applied.

Logic Table

Inputs			Outputs
CLR	**CE**	**C**	**Qz : Q0**
1	X	X	0
0	0	X	No Change
0	1	↓	Inc
z = bit width - 1			

Design Entry Method

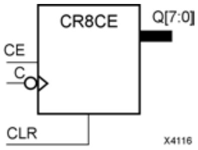
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CR8CE

Macro: 8-Bit Negative-Edge Binary Ripple Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is an 8-bit cascadable, clearable, binary, ripple counter with clock enable and asynchronous clear.

The asynchronous clear (CLR), when High, overrides all other inputs and causes the Q outputs to go to logic level zero. The counter increments when the clock enable input (CE) is High during the High-to-Low clock (C) transition. The counter ignores clock transitions when CE is Low.

Larger counters can be created by connecting the last Q output of the first stage to the clock input of the next stage. CLR and CE inputs are connected in parallel. The clock period is not affected by the overall length of a ripple counter. The overall clock-to-output propagation is $n(t_{C-Q})$, where n is the number of stages and the time t_{C-Q} is the C-to-Qz propagation delay of each stage.

This counter is asynchronously cleared, outputs Low, when power is applied.

Logic Table

Inputs			**Outputs**
CLR	**CE**	**C**	**Qz : Q0**
1	X	X	0
0	0	X	No Change
0	1	↓	Inc
z = bit width - 1			

Design Entry Method

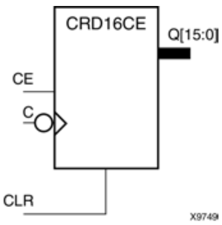
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CRD16CE

Macro: 16-Bit Dual-Edge Triggered Binary Ripple Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a dual edge triggered 16-bit cascadable, clearable, binary ripple counter.

The asynchronous clear (CLR), when High, overrides all other inputs and causes the Q outputs to go to logic level zero. The counter increments when the clock enable input (CE) is High during the High-to-Low and Low-to-High clock (C) transitions. The counter ignores clock transitions when CE is Low.

Larger counters can be created by connecting the last Q output of the first stage to the clock input of the next stage. CLR and CE inputs are connected in parallel. The clock period is not affected by the overall length of a ripple counter. The overall clock-to-output propagation is n(t_{C-Q}), where n is the number of stages and the time t_{C-Q} is the C-to-Qz propagation delay of each stage.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			Outputs
CLR	**CE**	**C**	**Qz : Q0**
1	X	X	0
0	0	X	No Change
0	1	↑	Inc
0	1	↓	Inc
z = bit width - 1			

Design Entry Method

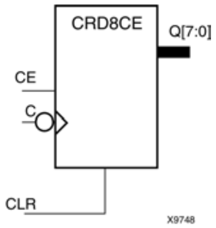
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

CRD8CE

Macro: 8-Bit Dual-Edge Triggered Binary Ripple Counter with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a dual edge triggered 8-bit cascadable, clearable, binary ripple counter.

The asynchronous clear (CLR), when High, overrides all other inputs and causes the Q outputs to go to logic level zero. The counter increments when the clock enable input (CE) is High during the High-to-Low and Low-to-High clock (C) transitions. The counter ignores clock transitions when CE is Low.

Larger counters can be created by connecting the last Q output of the first stage to the clock input of the next stage. CLR and CE inputs are connected in parallel. The clock period is not affected by the overall length of a ripple counter. The overall clock-to-output propagation is n(t_{C-Q}), where n is the number of stages and the time t_{C-Q} is the C-to-Qz propagation delay of each stage.

This counter is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			**Outputs**
CLR	**CE**	**C**	**Qz : Q0**
1	X	X	0
0	0	X	No Change
0	1	↑	Inc
0	1	↓	Inc
z = bit width - 1			

Design Entry Method

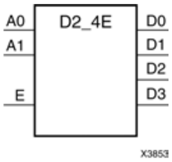
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

D2_4E

Macro: 2- to 4-Line Decoder/Demultiplexer with Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a decoder/demultiplexer. When the enable (E) input of this element is High, one of four active-High outputs (D3 : D0) is selected with a 2-bit binary address (A1 : A0) input. The non-selected outputs are Low. Also, when the E input is Low, all outputs are Low. In demultiplexer applications, the E input is the data input.

Logic Table

Inputs			Outputs			
A1	**A0**	**E**	**D3**	**D2**	**D1**	**D0**
X	X	0	0	0	0	0
0	0	1	0	0	0	1
0	1	1	0	0	1	0
1	0	1	0	1	0	0
1	1	1	1	0	0	0

Design Entry Method

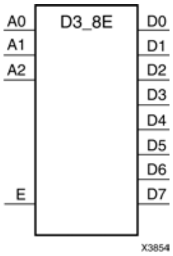
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

D3_8E

Macro: 3- to 8-Line Decoder/Demultiplexer with Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

When the enable (E) input of the D3_8E decoder/demultiplexer is High, one of eight active-High outputs (D7 : D0) is selected with a 3-bit binary address (A2 : A0) input. The non-selected outputs are Low. Also, when the E input is Low, all outputs are Low. In demultiplexer applications, the E input is the data input.

Logic Table

Inputs				**Outputs**							
A2	**A1**	**A0**	**E**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
X	X	X	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	1
0	0	1	1	0	0	0	0	0	0	1	0
0	1	0	1	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	1	0	0	0
1	0	0	1	0	0	0	1	0	0	0	0
1	0	1	1	0	0	1	0	0	0	0	0
1	1	0	1	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

Design Entry Method

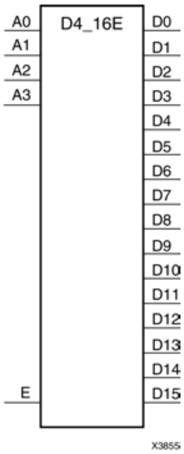
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

D4_16E

Macro: 4- to 16-Line Decoder/Demultiplexer with Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a decoder/demultiplexer. When the enable (E) input of this design element is High, one of 16 active-High outputs (D15 : D0) is selected with a 4-bit binary address (A3 : A0) input. The non-selected outputs are Low. Also, when the E input is Low, all outputs are Low. In demultiplexer applications, the E input is the data input.

Design Entry Method

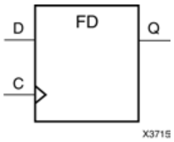
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FD

Macro: D Flip-Flop



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a D-type flip-flop with data input (D) and data output (Q). The data on the D inputs is loaded into the flip-flop during the Low-to-High clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs		Outputs
D	**C**	**Q**
0	↑	0
1	↑	1

Design Entry Method

This design element is only for use in schematics.

Available Attributes

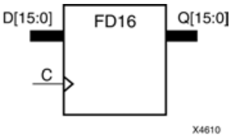
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FD16

Macro: Multiple D Flip-Flop



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a multiple D-type flip-flops with data inputs (D) and data outputs (Q), with a 16-bit register, each with a common clock (C). The data on the D inputs is loaded into the flip-flop during the Low-to-High clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs		Outputs
Dz : D0	**C**	**Qz : Q0**
0	↑	0
1	↑	1
z = bit-width - 1		

Design Entry Method

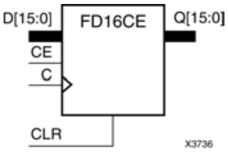
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FD16CE

Macro: 16-Bit Data Register with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 16-bit data register with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High clock (C) transition. When CLR is High, it overrides all other inputs and resets the data outputs (Q) Low. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				**Outputs**
CLR	**CE**	**Dz : D0**	**C**	**Qz : Q0**
1	X	X	X	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
z = bit-width - 1				

Design Entry Method

This design element is only for use in schematics.

Available Attributes

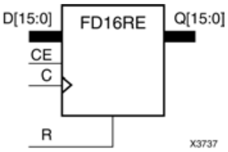
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	Any 16-bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FD16RE

Macro: 16-Bit Data Register with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 16-bit data registers. When the clock enable (CE) input is High, and the synchronous reset (R) input is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q0) during the Low-to-High clock (C) transition. When R is High, it overrides all other inputs and resets the data outputs (Q) Low on the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				Outputs
R	**CE**	**Dz : D0**	**C**	**Qz : Q0**
1	X	X	↑	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
z = bit-width - 1				

Design Entry Method

This design element is only for use in schematics.

Available Attributes

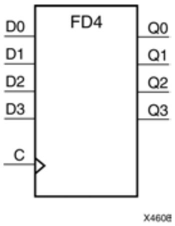
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	Any 16-bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FD4

Macro: Multiple D Flip-Flop



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a multiple D-type flip-flops with data inputs (D) and data outputs (Q), with a 4-bit register, each with a common clock (C). The data on the D inputs is loaded into the flip-flop during the Low-to-High clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs		Outputs
Dz : D0	**C**	**Qz : Q0**
0	↑	0
1	↑	1
z = bit-width - 1		

Design Entry Method

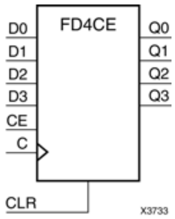
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FD4CE

Macro: 4-Bit Data Register with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 4-bit data register with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High clock (C) transition. When CLR is High, it overrides all other inputs and resets the data outputs (Q) Low. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				Outputs
CLR	**CE**	**Dz : D0**	**C**	**Qz : Q0**
1	X	X	X	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
z = bit-width - 1				

Design Entry Method

This design element is only for use in schematics.

Available Attributes

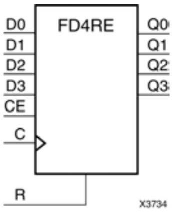
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	Any 4-Bit Value	All zeros	Sets the initial value of Q output after configuration.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FD4RE

Macro: 4-Bit Data Register with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 4-bit data registers. When the clock enable (CE) input is High, and the synchronous reset (R) input is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q0) during the Low-to-High clock (C) transition. When R is High, it overrides all other inputs and resets the data outputs (Q) Low on the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				Outputs
R	**CE**	**Dz : D0**	**C**	**Qz : Q0**
1	X	X	↑	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
z = bit-width - 1				

Design Entry Method

This design element is only for use in schematics.

Available Attributes

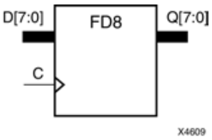
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	Any 4-Bit Value	All zeros	Sets the initial value of Q output after configuration.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FD8

Macro: Multiple D Flip-Flop



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a multiple D-type flip-flops with data inputs (D) and data outputs (Q), with a 8-bit register, each with a common clock (C). The data on the D inputs is loaded into the flip-flop during the Low-to-High clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs		**Outputs**
Dz : D0	**C**	**Qz : Q0**
0	↑	0
1	↑	1
z = bit-width - 1		

Design Entry Method

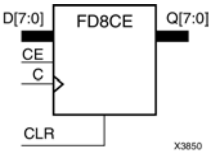
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FD8CE

Macro: 8-Bit Data Register with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 8-bit data register with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High clock (C) transition. When CLR is High, it overrides all other inputs and resets the data outputs (Q) Low. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				Outputs
CLR	**CE**	**Dz : D0**	**C**	**Qz : Q0**
1	X	X	X	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
z = bit-width - 1				

Design Entry Method

This design element is only for use in schematics.

Available Attributes

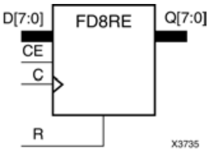
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	Any 8-Bit Value	All zeros	Sets the initial value of Q output after configuration.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FD8RE

Macro: 8-Bit Data Register with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is an 8-bit data register. When the clock enable (CE) input is High, and the synchronous reset (R) input is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q0) during the Low-to-High clock (C) transition. When R is High, it overrides all other inputs and resets the data outputs (Q) Low on the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				Outputs
R	**CE**	**Dz : D0**	**C**	**Qz : Q0**
1	X	X	↑	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
z = bit-width - 1				

Design Entry Method

This design element is only for use in schematics.

Available Attributes

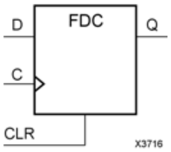
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	Any 8-Bit Value	All zeros	Sets the initial value of Q output after configuration.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDC

Macro: D Flip-Flop with Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single D-type flip-flop with data (D) and asynchronous clear (CLR) inputs and data output (Q). The asynchronous CLR, when High, overrides all other inputs and sets the (Q) output Low. The data on the (D) input is loaded into the flip-flop when CLR is Low on the Low-to-High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			Outputs
CLR	**D**	**C**	**Q**
1	X	X	0
0	D	↑	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

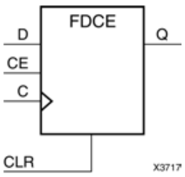
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration For Spartan®-6, the INIT value should always match the polarity of the set or reset. For this element, the INIT should be 0. If set to 1, an asynchronous circuit must be created to exhibit this behavior, which Xilinx does not recommend.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDCE

Primitive: D Flip-Flop with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single D-type flip-flop with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data input (D) of this design element is transferred to the corresponding data output (Q) during the Low-to-High clock (C) transition. When CLR is High, it overrides all other inputs and resets the data output (Q) Low. When CE is Low, clock transitions are ignored.

For XC9500XL and XC9500XV devices, logic connected to the clock enable (CE) input may be implemented using the clock enable product term (p-term) in the macrocell, provided the logic can be completely implemented using the single p-term available for clock enable without requiring feedback from another macrocell. Only FDCE and FDPE flip-flops may take advantage of the clock-enable p-term.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				**Outputs**
CLR	**CE**	**D**	**C**	**Q**
1	X	X	X	0
0	0	X	X	No Change
0	1	D	↑	D

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration For Spartan®-6, the INIT value should always match the polarity of the set or reset. For this element, the INIT should be 0. If set to 1, an asynchronous circuit must be created to exhibit this behavior, which Xilinx does not recommend.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- FDCE: Single Data Rate D Flip-Flop with Asynchronous Clear and
--       Clock Enable (posedge clk).  All families.
-- Xilinx HDL Libraries Guide, version 11.2

FDCE_inst : FDCE
generic map (
   INIT => '0') -- Initial value of register ('0' or '1')
port map (
   Q => Q,       -- Data output
   C => C,       -- Clock input
   CE => CE,     -- Clock enable input
   CLR => CLR,   -- Asynchronous clear input
   D => D        -- Data input
);

-- End of FDCE_inst instantiation
```

Verilog Instantiation Template

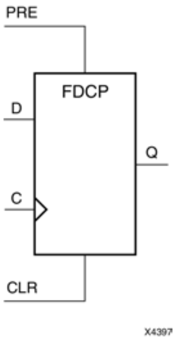
```
// FDCE: Single Data Rate D Flip-Flop with Asynchronous Clear and
//       Clock Enable (posedge clk).
//       All families.
// Xilinx HDL Libraries Guide, version 11.2

FDCE #(
   .INIT(1'b0) // Initial value of register (1'b0 or 1'b1)
) FDCE_inst (
   .Q(Q),      // Data output
   .C(C),      // Clock input
   .CE(CE),    // Clock enable input
   .CLR(CLR),  // Asynchronous clear input
   .D(D)       // Data input
);

// End of FDCE_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDCP

Primitive: D Flip-Flop with Asynchronous Preset and Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single D-type flip-flop with data (D), asynchronous preset (PRE) and clear (CLR) inputs, and data output (Q). The asynchronous PRE, when High, sets the (Q) output High; CLR, when High, resets the output Low. Data on the (D) input is loaded into the flip-flop when PRE and CLR are Low on the Low-to-High clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				Outputs
CLR	**PRE**	**D**	**C**	**Q**
1	X	X	X	0
0	1	X	X	1
0	0	D	↑	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

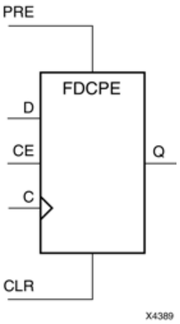
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDCPE

Primitive: D Flip-Flop with Clock Enable and Asynchronous Preset and Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single D-type flip-flop with data (D), clock enable (CE), asynchronous preset (PRE), and asynchronous clear (CLR) inputs. The asynchronous active high PRE sets the Q output High; that active high CLR resets the output Low and has precedence over the PRE input. Data on the D input is loaded into the flip-flop when PRE and CLR are Low and CE is High on the Low-to-High clock (C) transition. When CE is Low, the clock transitions are ignored and the previous value is retained. The FDCPE is generally implemented as a slice or IOB register within the device.

For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net. For FPGA devices, upon power-up, the initial value of this component is specified by the INIT attribute. If a subsequent GSR (Global Set/Reset) is asserted, the flop is asynchronously set to the INIT value.

Note While this device supports the use of asynchronous set and reset, it is not generally recommended to be used for in most cases. Use of asynchronous signals pose timing issues within the design that are difficult to detect and control and also have an adverse affect on logic optimization causing a larger design that can consume more power than if a synchronous set or reset is used.

Logic Table

Inputs					Outputs
CLR	**PRE**	**CE**	**D**	**C**	**Q**
1	X	X	X	X	0
0	1	X	X	X	1
0	0	0	X	X	No Change
0	0	1	D	↑	D

Port Descriptions

Port	Direction	Width	Function
Q	Output	1	Data output
C	Input	1	Clock input
CE	Input	1	Clock enable input
CLR	Input	1	Asynchronous clear input
D	Input	1	Data input
PRE	Input	1	Asynchronous set input

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0,1	0	Sets the initial value of Q output after configuration and on GSR.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- FDCPE: Single Data Rate D Flip-Flop with Asynchronous Clear, Set and
--        Clock Enable (posedge clk).
--        Virtex-4/5, Spartan-3/3E/3A/3A DSP
-- Xilinx HDL Libraries Guide, version 11.2

FDCPE_inst : FDCPE
generic map (
   INIT => '0') -- Initial value of register ('0' or '1')
port map (
   Q => Q,      -- Data output
   C => C,      -- Clock input
   CE => CE,    -- Clock enable input
   CLR => CLR,  -- Asynchronous clear input
   D => D,      -- Data input
   PRE => PRE   -- Asynchronous set input
);

-- End of FDCPE_inst instantiation
```

Verilog Instantiation Template

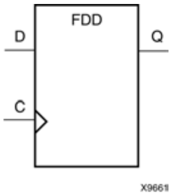
```
// FDCPE: Single Data Rate D Flip-Flop with Asynchronous Clear, Set and
//        Clock Enable (posedge clk).
//        Virtex-4/5, Spartan-3/3E/3A/3A DSP
// Xilinx HDL Libraries Guide, version 11.2

FDCPE #(
   .INIT(1'b0) // Initial value of register (1'b0 or 1'b1)
) FDCPE_inst (
   .Q(Q),      // Data output
   .C(C),      // Clock input
   .CE(CE),    // Clock enable input
   .CLR(CLR),  // Asynchronous clear input
   .D(D),      // Data input
   .PRE(PRE)   // Asynchronous set input
);

// End of FDCPE_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDD

Macro: Dual Edge Triggered D Flip-Flop



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a single dual edge triggered D-type flip-flop with data input (D) and data output (Q). The data on the D input is loaded into the flip-flop during the Low-to-High and the High-to-Low clock (C) transitions.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs		Outputs
D	**C**	**Q**
0	↑	0
1	↑	1
0	↓	0
1	↓	1

Design Entry Method

This design element is only for use in schematics.

Available Attributes

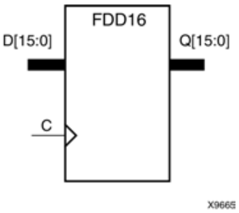
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDD16

Macro: Multiple Dual Edge Triggered D Flip-Flop



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a multiple dual edge triggered D-type flip-flop with data inputs (D) and data outputs (Q). It is a 16-bit register with a common clock (C). The data on the D inputs is loaded into the flip-flop during the Low-to-High and High-to-Low clock (C) transitions.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs		Outputs
Dz : D0	**C**	**Qz : Q0**
0	↑	0
1	↑	1
0	↓	0
1	↓	1
z = bit-width - 1		

Design Entry Method

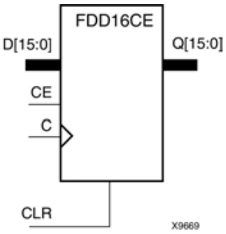
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDD16CE

Macro: 16-Bit Dual Edge Triggered Data Register with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a 16-bit data registers with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High and High-to-Low clock (C) transitions. When CLR is High, it overrides all other inputs and resets the data outputs (Q) Low. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				**Outputs**
CLR	**CE**	**Dz : D0**	**C**	**Qz : Q0**
1	X	X	X	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
0	1	Dn	↓	Dn
z = bit-width - 1				

Design Entry Method

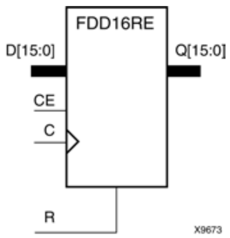
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDD16RE

Macro: 16-Bit Dual Edge Triggered Data Register with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a 16-bit data register. When the clock enable (CE) input is High, and the synchronous reset (R) input is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q0) during the Low-to-High or High-to-Low clock (C) transition. When R is High, it overrides all other inputs and resets the data outputs (Q) Low on the Low-to-High and High-to-Low clock transitions. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				Outputs
R	**CE**	**Dz : D0**	**C**	**Qz : Q0**
1	X	X	↑	0
1	X	X	↓	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
0	1	Dn	↓	Dn
z = bit-width - 1				

Design Entry Method

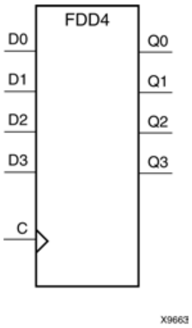
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDD4

Multiple Dual Edge Triggered D Flip-Flop



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a multiple dual edge triggered D-type flip-flop with data inputs (D) and data outputs (Q). It is a 4-bit register with a common clock (C). The data on the D inputs is loaded into the flip-flop during the Low-to-High and High-to-Low clock (C) transitions.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs		Outputs
Dz : D0	**C**	**Qz : Q0**
0	↑	0
1	↑	1
0	↓	0
1	↓	1
z = bit-width - 1		

Design Entry Method

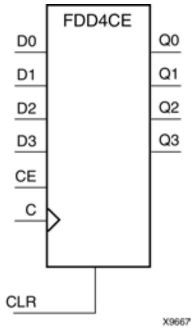
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDD4CE

Macro: 4-Bit Dual Edge Triggered Data Register with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a 4-bit data registers with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High and High-to-Low clock (C) transitions. When CLR is High, it overrides all other inputs and resets the data outputs (Q) Low. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				Outputs
CLR	**CE**	**Dz : D0**	**C**	**Qz : Q0**
1	X	X	X	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
0	1	Dn	↓	Dn
z = bit-width - 1				

Design Entry Method

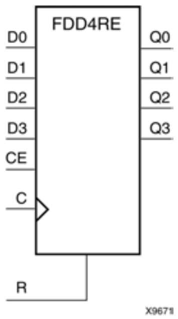
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDD4RE

Macro: 4-Bit Dual Edge Triggered Data Register with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a 4-bit data register. When the clock enable (CE) input is High, and the synchronous reset (R) input is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q0) during the Low-to-High or High-to-Low clock (C) transition. When R is High, it overrides all other inputs and resets the data outputs (Q) Low on the Low-to-High and High-to-Low clock transitions. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				Outputs
R	**CE**	**Dz : D0**	**C**	**Qz : Q0**
1	X	X	↑	0
1	X	X	↓	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
0	1	Dn	↓	Dn
z = bit-width - 1				

Design Entry Method

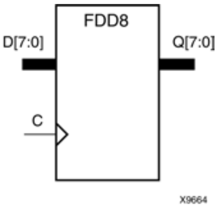
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDD8

Macro: Multiple Dual Edge Triggered D Flip-Flop



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a multiple dual edge triggered D-type flip-flop with data inputs (D) and data outputs (Q). It is an 8-bit register with a common clock (C). The data on the D inputs is loaded into the flip-flop during the Low-to-High and High-to-Low clock (C) transitions.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs		**Outputs**
Dz : D0	**C**	**Qz : Q0**
0	↑	0
1	↑	1
0	↓	0
1	↓	1
z = bit-width - 1		

Design Entry Method

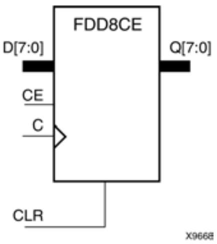
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDD8CE

Macro: 8-Bit Dual Edge Triggered Data Register with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a 8-bit data registers with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High and High-to-Low clock (C) transitions. When CLR is High, it overrides all other inputs and resets the data outputs (Q) Low. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				Outputs
CLR	**CE**	**Dz : D0**	**C**	**Qz : Q0**
1	X	X	X	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
0	1	Dn	↓	Dn
z = bit-width - 1				

Design Entry Method

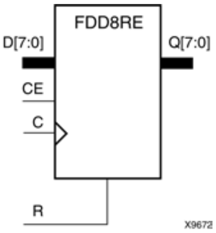
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDD8RE

Macro: 8-Bit Dual Edge Triggered Data Register with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a 8-bit data register. When the clock enable (CE) input is High, and the synchronous reset (R) input is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q0) during the Low-to-High or High-to-Low clock (C) transition. When R is High, it overrides all other inputs and resets the data outputs (Q) Low on the Low-to-High and High-to-Low clock transitions. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				**Outputs**
R	**CE**	**Dz : D0**	**C**	**Qz : Q0**
1	X	X	↑	0
1	X	X	↓	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
0	1	Dn	↓	Dn
z = bit-width - 1				

Design Entry Method

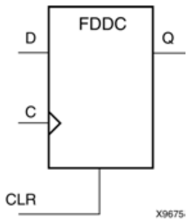
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDDC

Macro: D Dual Edge Triggered Flip-Flop with Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a single dual edge triggered D-type flip-flop with data (D) and asynchronous clear (CLR) inputs and data output (Q). The asynchronous CLR, when High, overrides all other inputs and sets the Q output Low. The data on the D input is loaded into the flip-flop when CLR is Low on the Low-to-High and High-to-Low clock (C) transitions.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			Outputs
CLR	**D**	**C**	**Q**
1	X	X	0
0	1	↑	1
0	1	↓	1
0	0	↑	0
0	0	↓	0

Design Entry Method

This design element is only for use in schematics.

Available Attributes

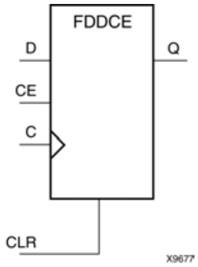
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDDCE

Primitive: Dual Edge Triggered D Flip-Flop with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a single dual edge triggered D-type flip-flop with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data input (D) of FDDCE is transferred to the corresponding data output (Q) during the Low-to-High and High-to-Low clock (C) transitions. When CLR is High, it overrides all other inputs and resets the data output (Q) Low. When CE is Low, clock transitions are ignored.

Logic connected to the clock enable (CE) input may be implemented using the clock enable product term (p-term) in the macrocell, provided the logic can be completely implemented using the single p-term available for clock enable without requiring feedback from another macrocell. Only FDDCE and FDDPE flip-flops can take advantage of the clock-enable p-term.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				Outputs
CLR	**CE**	**D**	**C**	**Q**
1	X	X	X	0
0	0	X	X	No Change
0	1	1	↑	1
0	1	0	↑	0
0	1	1	↓	1
0	1	0	↓	0

Design Entry Method

This design element is only for use in schematics.

Available Attributes

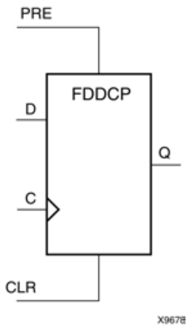
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDDCP

Primitive: Dual Edge Triggered D Flip-Flop Asynchronous Preset and Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a single dual edge triggered D-type flip-flop with data (D), asynchronous preset (PRE) and clear (CLR) inputs, and data output (Q). The asynchronous PRE, when High, sets the Q output High; CLR, when High, resets the output Low. Data on the D input is loaded into the flip-flop when PRE and CLR are Low on the Low-to-High and High-to-Low clock (C) transitions.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				Outputs
CLR	**PRE**	**D**	**C**	**Q**
1	X	X	X	0
0	1	X	X	1
0	0	0	↑	0
0	0	1	↑	1
0	0	0	↓	0
0	0	1	↓	1

Design Entry Method

This design element is only for use in schematics.

Available Attributes

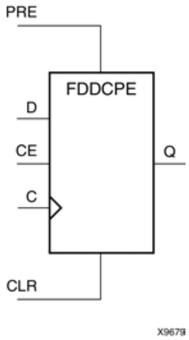
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDDCPE

Macro: Dual Edge Triggered D Flip-Flop with Clock Enable and Asynchronous Preset and Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a single dual edge triggered D-type flip-flop with data (D), clock enable (CE), asynchronous preset (PRE), and asynchronous clear (CLR) inputs and data output (Q). The asynchronous PRE, when High, sets the Q output High; CLR, when High, resets the output Low. Data on the D input is loaded into the flip-flop when PRE and CLR are Low and CE is High on the Low-to-High and High-to-Low clock (C) transitions. When CE is Low, the clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					Outputs
CLR	**PRE**	**CE**	**D**	**C**	**Q**
1	X	X	X	X	0
0	1	X	X	X	1
0	0	0	X	X	No Change
0	0	1	0	↑	0
0	0	1	1	↑	1
0	0	1	0	↓	0
0	0	1	1	↓	1

Design Entry Method

This design element is only for use in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- FDDCPE: Double Data Rate Register with Asynchronous Clear and Set
--         and Clock Enable (Clear has priority).  CoolRunner-II
-- Xilinx HDL Language Template, version 10.1

FDDCPE_inst : FDDCPE
port map (
   Q => Q,      -- Data output
   C => C,      -- Clock input
   CE => CE,    -- Clock enable input
   CLR => CLR,  -- Asynchronous clear input
   D => D,      -- Data input
   PRE => PRE   -- Asynchronous set input
);

-- End of FDDCPE_inst instantiation
```

Verilog Instantiation Template

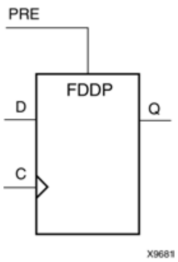
```
// FDDCPE: Double Data Rate Register with Asynchronous Clear and Set
//         and Clock Enable (Clear has priority).
//         CoolRunner-II
// Xilinx HDL Language Template, version 10.1

FDDCPE FDDCPE_inst (
   .Q(Q),      // Data output
   .C(C),      // Clock input
   .CE(CE),    // Clock enable input
   .CLR(CLR),  // Asynchronous clear input
   .D(D),      // Data input
   .PRE(PRE)   // Asynchronous set input
);

// End of FDDCPE_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDDP

Macro: Dual Edge Triggered D Flip-Flop with Asynchronous Preset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a single dual edge triggered D-type flip-flop with data (D) and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and presets the Q output High. The data on the D input is loaded into the flip-flop when PRE is Low on the Low-to-High and High-to-Low clock (C) transitions.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			Outputs
PRE	**C**	**D**	**Q**
1	X	X	1
0	↑	1	1
0	↑	0	0
0	↓	1	1
0	↓	0	0

Design Entry Method

This design element is only for use in schematics.

Available Attributes

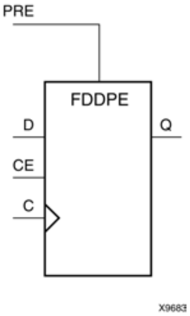
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDDPE

Primitive: Dual Edge Triggered D Flip-Flop with Clock Enable and Asynchronous Preset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a single dual edge triggered D-type flip-flop with data (D), clock enable (CE), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and sets the Q output High. Data on the D input is loaded into the flip-flop when PRE is Low and CE is High on the Low-to-High and High-to-Low clock (C) transitions. When CE is Low, the clock transitions are ignored.

Logic connected to the clock enable (CE) input may be implemented using the clock enable product term (p-term) in the macrocell, provided the logic can be completely implemented using the single p-term available for clock enable without requiring feedback from another macrocell. Only FDDCE and FDDPE flip-flops primitives may take advantage of the clock-enable p-term.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				**Outputs**
PRE	**CE**	**D**	**C**	**Q**
1	X	X	X	1
0	0	X	X	No Change
0	1	0	↑	0
0	1	1	↑	1
0	1	0	↓	0
0	1	1	↓	1

Design Entry Method

This design element is only for use in schematics.

Available Attributes

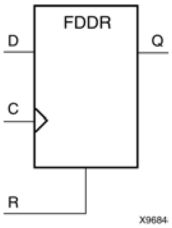
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDDR

Macro: Dual Edge Triggered D Flip-Flop with Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a single dual edge triggered D-type flip-flop with data (D) and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the Q output Low on the Low-to-High and High-to-Low clock (C) transitions. The data on the D input is loaded into the flip-flop when R is Low during the Low-to-High or High-to-Low clock transitions.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			Outputs
R	**D**	**C**	**Q**
1	X	↑	0
1	X	↓	0
0	1	↑	1
0	0	↑	0
0	1	↓	1
0	0	↓	0

Design Entry Method

This design element is only for use in schematics.

Available Attributes

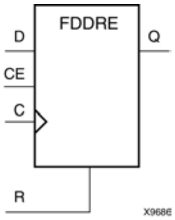
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDDRE

Macro: Dual Edge Triggered D Flip-Flop with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

FDDRE is a single dual edge triggered D-type flip-flop with data (D), clock enable (CE), and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the Q output Low on the Low-to-High or High-to-Low clock (C) transition. The data on the D input is loaded into the flip-flop when R is Low and CE is High during the Low-to-High and High-to-Low clock transitions.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				**Outputs**
R	**CE**	**D**	**C**	**Q**
1	X	X	↑	0
1	X	X	↓	0
0	0	X	X	No Change
0	1	1	↑	1
0	1	0	↑	0
0	1	1	↓	1
0	1	0	↓	0

Design Entry Method

This design element can be used in schematics.

Available Attributes

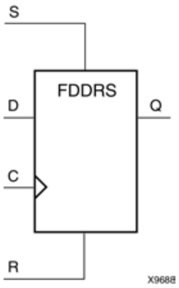
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDDRS

Macro: Dual Edge Triggered D Flip-Flop with Synchronous Reset and Set



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

FDDRS is a single dual edge triggered D-type flip-flop with data (D), synchronous set (S), and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the Q output Low during the Low-to-High or High-to-Low clock (C) transitions. (Reset has precedence over Set.) When S is High and R is Low, the flip-flop is set, output High, during the Low-to-High or High-to-Low clock transition. When R and S are Low, data on the (D) input is loaded into the flip-flop during the Low-to-High and High-to-Low clock transitions.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				Outputs
R	S	D	C	Q
1	X	X	↑	0
1	X	X	↓	0
0	1	X	↑	1
0	1	X	↓	1
0	0	1	↑	1
0	0	1	↓	1
0	0	0	↑	0
0	0	0	↓	0

Design Entry Method

This design element is only for use in schematics.

Available Attributes

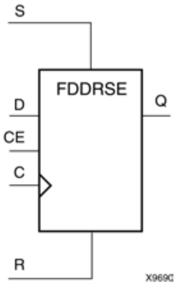
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDDRSE

Macro: Dual Edge Triggered D Flip-Flop with Synchronous Reset and Set and Clock Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

FDDRSE is a single dual edge triggered D-type flip-flop with synchronous reset (R), synchronous set (S), and clock enable (CE) inputs and data output (Q). The reset (R) input, when High, overrides all other inputs and resets the Q output Low during the Low-to-High or High-to-Low clock transitions. (Reset has precedence over Set.) When the set (S) input is High and R is Low, the flip-flop is set, output High, during the Low-to-High or High-to-Low clock (C) transition. Data on the D input is loaded into the flip-flop when R and S are Low and CE is High during the Low-to-High and High-to-Low clock transitions.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					**Outputs**
R	**S**	**CE**	**D**	**C**	**Q**
1	X	X	X	↑	0
1	X	X	X	↓	0
0	1	X	X	↑	1
0	1	X	X	↓	1
0	0	0	X	X	No Change
0	0	1	1	↑	1
0	0	1	0	↑	0
0	0	1	1	↓	1
0	0	1	0	↓	0

Design Entry Method

This design element is only for use in schematics.

Available Attributes

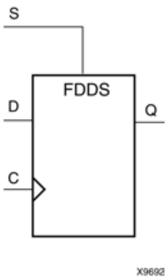
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDDS

Macro: Dual Edge Triggered D Flip-Flop with Synchronous Set



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

FDDS is a single dual edge triggered D-type flip-flop with data (D) and synchronous set (S) inputs and data output (Q). The synchronous set input, when High, sets the Q output High on the Low-to-High or High-to-Low clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low during the Low-to-High and High-to-Low clock (C) transitions.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			Outputs
S	**D**	**C**	**Q**
1	X	↑	1
1	X	↓	1
0	1	↑	1
0	0	↑	0
0	1	↓	1
0	0	↓	0

Design Entry Method

This design element is only for use in schematics.

Available Attributes

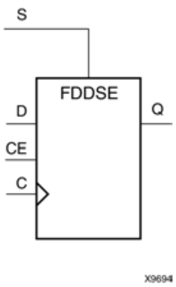
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDDSE

Macro: D Flip-Flop with Clock Enable and Synchronous Set



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

FDDSE is a single dual edge triggered D-type flip-flop with data (D), clock enable (CE), and synchronous set (S) inputs and data output (Q). The synchronous set (S) input, when High, overrides the clock enable (CE) input and sets the Q output High during the Low-to-High or High-to-Low clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low and CE is High during the Low-to-High and High-to-Low clock (C) transitions.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				Outputs
S	**CE**	**D**	**C**	**Q**
1	X	X	↑	1
1	X	X	↓	1
0	0	X	X	No Change
0	1	1	↑	1
0	1	0	↑	0
0	1	1	↓	1
0	1	0	↓	0

Design Entry Method

This design element is only for use in schematics.

Available Attributes

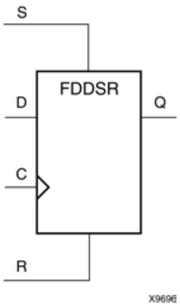
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDDSR

Macro: Dual Edge Triggered D Flip-Flop with Synchronous Set and Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

FDDSR is a single dual edge triggered D-type flip-flop with data (D), synchronous reset (R) and synchronous set (S) inputs and data output (Q). When the set (S) input is High, it overrides all other inputs and sets the Q output High during the Low-to-High or High-to-Low clock transition. (Set has precedence over Reset.) When reset (R) is High and S is Low, the flip-flop is reset, output Low, on the Low-to-High or High-to-Low clock transition. Data on the D input is loaded into the flip-flop when S and R are Low on the Low-to-High and High-to-Low clock transitions.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				Outputs
S	**R**	**D**	**C**	**Q**
1	X	X	↑	1
1	X	X	↓	1
0	1	X	↑	0
0	1	X	↓	0
0	0	1	↑	1
0	0	0	↑	0
0	0	1	↓	1
0	0	0	↓	0

Design Entry Method

This design element is only for use in schematics.

Available Attributes

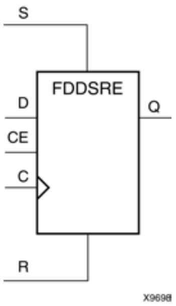
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDDSRE

Macro: Dual Edge Triggered D Flip-Flop with Synchronous Set and Reset and Clock Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

FDDSRE is a single dual edge triggered D-type flip-flop with synchronous set (S), synchronous reset (R), and clock enable (CE) inputs and data output (Q). When synchronous set (S) is High, it overrides all other inputs and sets the Q output High during the Low-to-High or High-to-Low clock transition. (Set has precedence over Reset.) When synchronous reset (R) is High and S is Low, output Q is reset Low during the Low-to-High or High-to-Low clock transition. Data is loaded into the flip-flop when S and R are Low and CE is High during the Low-to-High and High-to-Low clock transitions. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					Outputs
S	**R**	**CE**	**D**	**C**	**Q**
1	X	X	X	↑	1
1	X	X	X	↓	1
0	1	X	X	↑	0
0	1	X	X	↓	0
0	0	0	X	X	No Change
0	0	1	1	↑	1
0	0	1	0	↑	0
0	0	1	1	↓	1
0	0	1	0	↓	0

Design Entry Method

This design element is only for use in schematics.

Available Attributes

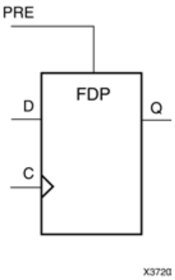
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDP

Macro: D Flip-Flop with Asynchronous Preset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single D-type flip-flop with data (D) and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and presets the (Q) output High. The data on the (D) input is loaded into the flip-flop when PRE is Low on the Low-to-High clock (C) transition.

For CPLD devices, this flip-flop is asynchronously cleared, output Low, when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			Outputs
PRE	**C**	**D**	**Q**
1	X	X	1
0	↑	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

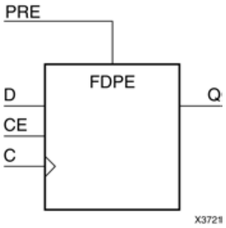
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration For Spartan®-6, Xilinx recommends that the INIT value always matches the polarity of the set or reset. For this element, the INIT should be 1. If set to 0, additional asynchronous circuitry will be created to correctly model the behavior.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDPE

Primitive: D Flip-Flop with Clock Enable and Asynchronous Preset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single D-type flip-flop with data (D), clock enable (CE), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and sets the (Q) output High. Data on the (D) input is loaded into the flip-flop when PRE is Low and CE is High on the Low-to-High clock (C) transition. When CE is Low, the clock transitions are ignored.

For CPLD devices, this flip-flop is asynchronously cleared, output Low, when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				**Outputs**
PRE	**CE**	**D**	**C**	**Q**
1	X	X	X	1
0	0	X	X	No Change
0	1	D	↑	D

Design Entry Method

This design element can be used in schematics.

Available Attributes

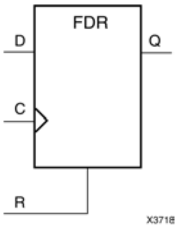
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration For Spartan®-6, Xilinx recommends that the INIT value always matches the polarity of the set or reset. For this element, the INIT should be 1. If set to 0, additional asynchronous circuitry will be created to correctly model the behavior.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDR

Macro: D Flip-Flop with Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single D-type flip-flop with data (D) and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the (Q) output Low on the Low-to-High clock (C) transition. The data on the (D) input is loaded into the flip-flop when R is Low during the Low-to- High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			Outputs
R	**D**	**C**	**Q**
1	X	↑	0
0	D	↑	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

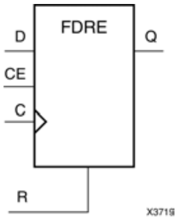
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDRE

Macro: D Flip-Flop with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single D-type flip-flop with data (D), clock enable (CE), and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the (Q) output Low on the Low-to-High clock (C) transition. The data on the (D) input is loaded into the flip-flop when R is Low and CE is High during the Low-to-High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				Outputs
R	**CE**	**D**	**C**	**Q**
1	X	X	↑	0
0	0	X	X	No Change
0	1	D	↑	D

Design Entry Method

This design element can be used in schematics.

Available Attributes

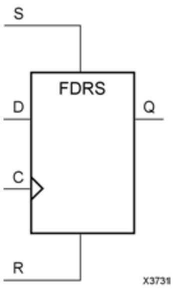
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration For Spartan®-6, the INIT value should always match the polarity of the set or reset. For this element, the INIT should be 0. If set to 1, an asynchronous circuit must be created to exhibit this behavior, which Xilinx does not recommend.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDRS

Macro: D Flip-Flop with Synchronous Reset and Set



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

FDRS is a single D-type flip-flop with data (D), synchronous set (S), and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the (Q) output Low during the Low-to-High clock (C) transition. (Reset has precedence over Set.) When S is High and R is Low, the flip-flop is set, output High, during the Low-to-High clock transition. When R and S are Low, data on the (D) input is loaded into the flip-flop during the Low-to-High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				Outputs
R	**S**	**D**	**C**	**Q**
1	X	X	↓	0
0	1	X	↓	1
0	0	D	↓	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

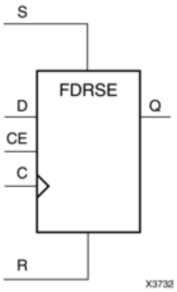
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDRSE

Macro: D Flip-Flop with Synchronous Reset and Set and Clock Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

FDRSE is a single D-type flip-flop with synchronous reset (R), synchronous set (S), clock enable (CE) inputs. The reset (R) input, when High, overrides all other inputs and resets the Q output Low during the Low-to-High clock transition. (Reset has precedence over Set.) When the set (S) input is High and R is Low, the flip-flop is set, output High, during the Low-to-High clock (C) transition. Data on the D input is loaded into the flip-flop when R and S are Low and CE is High during the Low-to-High clock transition.

Upon power-up, the initial value of this component is specified by the INIT attribute. If a subsequent GSR (Global Set/Reset) is asserted, the flop is asynchronously set to the INIT value.

Logic Table

Inputs					Outputs
R	**S**	**CE**	**D**	**C**	**Q**
1	X	X	X	↑	0
0	1	X	X	↑	1
0	0	0	X	X	No Change
0	0	1	1	↑	1
0	0	1	0	↑	0

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0,1	0	Sets the initial value of Q output after configuration and on GSR.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- FDRSE: Single Data Rate D Flip-Flop with Synchronous Clear, Set and
--        Clock Enable (posedge clk).
--        Virtex-4/5, Spartan-3/3E/3A/3A DSP
-- Xilinx HDL Libraries Guide, version 11.2

FDRSE_inst : FDRSE
generic map (
   INIT => '0') -- Initial value of register ('0' or '1')
port map (
   Q => Q,      -- Data output
   C => C,      -- Clock input
   CE => CE,    -- Clock enable input
   D => D,      -- Data input
   R => R,      -- Synchronous reset input
   S => S       -- Synchronous set input
);

-- End of FDRSE_inst instantiation
```

Verilog Instantiation Template

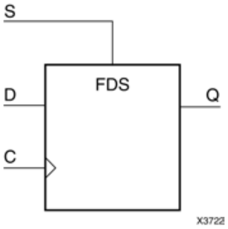
```
// FDRSE: Single Data Rate D Flip-Flop with Synchronous Clear, Set and
//        Clock Enable (posedge clk).
//        Virtex-4/5, Spartan-3/3E/3A/3A DSP
// Xilinx HDL Libraries Guide, version 11.2

FDRSE #(
   .INIT(1'b0) // Initial value of register (1'b0 or 1'b1)
) FDRSE_inst (
   .Q(Q),      // Data output
   .C(C),      // Clock input
   .CE(CE),    // Clock enable input
   .D(D),      // Data input
   .R(R),      // Synchronous reset input
   .S(S)       // Synchronous set input
);

// End of FDRSE_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDS

Macro: D Flip-Flop with Synchronous Set



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

FDS is a single D-type flip-flop with data (D) and synchronous set (S) inputs and data output (Q). The synchronous set input, when High, sets the Q output High on the Low-to-High clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low during the Low-to-High clock (C) transition.

For CPLD devices, this flip-flop is asynchronously cleared, output Low, when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			Outputs
S	**D**	**C**	**Q**
1	X	↑	1
0	D	↑	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

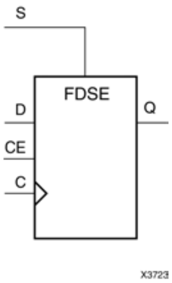
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDSE

Macro: D Flip-Flop with Clock Enable and Synchronous Set



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

FDSE is a single D-type flip-flop with data (D), clock enable (CE), and synchronous set (S) inputs and data output (Q). The synchronous set (S) input, when High, overrides the clock enable (CE) input and sets the Q output High during the Low-to-High clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low and CE is High during the Low-to-High clock (C) transition.

For CPLD devices, this flip-flop is asynchronously cleared, output Low, when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				Outputs
S	**CE**	**D**	**C**	**Q**
1	X	X	↑	1
0	0	X	X	No Change
0	1	D	↑	D

Design Entry Method

This design element can be used in schematics.

Available Attributes

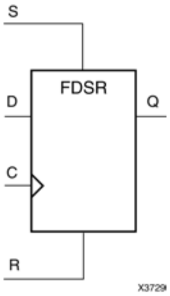
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration For Spartan®-6, Xilinx recommends that the INIT value always matches the polarity of the set or reset. For this element, the INIT should be 1. If set to 0, additional asynchronous circuitry will be created to correctly model the behavior.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDSR

D Flip-Flop with Synchronous Set and Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

FDSR is a single D-type flip-flop with data (D), synchronous reset (R) and synchronous set (S) inputs and data output (Q). When the set (S) input is High, it overrides all other inputs and sets the Q output High during the Low-to-High clock transition. (Set has precedence over Reset.) When reset (R) is High and S is Low, the flip-flop is reset, output Low, on the Low-to-High clock transition. Data on the D input is loaded into the flip-flop when S and R are Low on the Low-to-High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				Outputs
S	**R**	**D**	**C**	**Q**
1	X	X	↑	1
0	1	X	↑	0
0	0	1	↑	1
0	0	0	↑	0

Design Entry Method

This design element is only for use in schematics.

Available Attributes

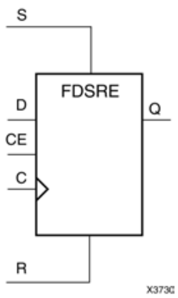
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FDSRE

Macro: D Flip-Flop with Synchronous Set and Reset and Clock Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

FDSRE is a single D-type flip-flop with synchronous set (S), synchronous reset (R), and clock enable (CE) inputs and data output (Q). When synchronous set (S) is High, it overrides all other inputs and sets the Q output High during the Low-to-High clock transition. (Set has precedence over Reset.) When synchronous reset (R) is High and S is Low, output Q is reset Low during the Low-to-High clock transition. Data is loaded into the flip-flop when S and R are Low and CE is High during the Low-to-high clock transition. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					Outputs
S	**R**	**CE**	**D**	**C**	**Q**
1	X	X	X	↑	1
0	1	X	X	↑	0
0	0	0	X	X	No Change
0	0	1	1	↑	1
0	0	1	0	↑	0

Design Entry Method

This design element is only for use in schematics.

Available Attributes

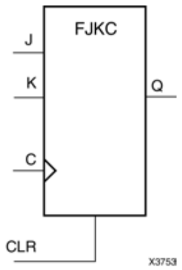
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FJKC

Macro: J-K Flip-Flop with Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single J-K-type flip-flop with J, K, and asynchronous clear (CLR) inputs and data output (Q). The asynchronous clear (CLR) input, when High, overrides all other inputs and resets the Q output Low. When CLR is Low, the output responds to the state of the J and K inputs, as shown in the following logic table, during the Low-to-High clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				**Outputs**
CLR	**J**	**K**	**C**	**Q**
1	X	X	X	0
0	0	0	↑	No Change
0	0	1	↑	0
0	1	0	↑	1
0	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

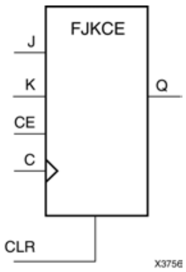
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration For Spartan®-6, the INIT value should always match the polarity of the set or reset. For this element, the INIT should be 0. If set to 1, an asynchronous circuit must be created to exhibit this behavior, which Xilinx does not recommend.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FJKCE

Macro: J-K Flip-Flop with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single J-K-type flip-flop with J, K, clock enable (CE), and asynchronous clear (CLR) inputs and data output (Q). The asynchronous clear (CLR), when High, overrides all other inputs and resets the Q output Low. When CLR is Low and CE is High, Q responds to the state of the J and K inputs, as shown in the following logic table, during the Low-to-High clock transition. When CE is Low, the clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					Outputs
CLR	**CE**	**J**	**K**	**C**	**Q**
1	X	X	X	X	0
0	0	X	X	X	No Change
0	1	0	0	X	No Change
0	1	0	1	↑	0
0	1	1	0	↑	1
0	1	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

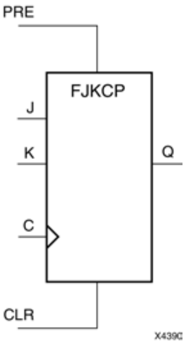
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration For Spartan®-6, the INIT value should always match the polarity of the set or reset. For this element, the INIT should be 0. If set to 1, an asynchronous circuit must be created to exhibit this behavior, which Xilinx does not recommend.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FJKCP

Macro: J-K Flip-Flop with Asynchronous Clear and Preset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single J-K-type flip-flop with J, K, asynchronous clear (CLR), and asynchronous preset (PRE) inputs and data output (Q). When the asynchronous clear (CLR) is High, all other inputs are ignored and Q is reset 0. The asynchronous preset (PRE), when High, and CLR set to Low overrides all other inputs and sets the Q output High. When CLR and PRE are Low, Q responds to the state of the J and K inputs during the Low-to-High clock transition, as shown in the following logic table.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					Outputs
CLR	**PRE**	**J**	**K**	**C**	**Q**
1	X	X	X	X	0
0	1	X	X	X	1
0	0	0	0	X	No Change
0	0	0	1	↑	0
0	0	1	0	↑	1
0	0	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

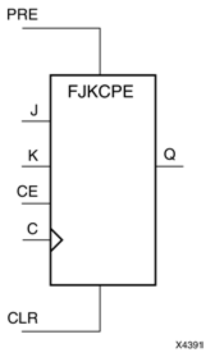
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FJKCPE

Macro: J-K Flip-Flop with Asynchronous Clear and Preset and Clock Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single J-K-type flip-flop with J, K, asynchronous clear (CLR), asynchronous preset (PRE), and clock enable (CE) inputs and data output (Q). When the asynchronous clear (CLR) is High, all other inputs are ignored and Q is reset 0. The asynchronous preset (PRE), when High, and CLR set to Low overrides all other inputs and sets the Q output High. When CLR and PRE are Low and CE is High, Q responds to the state of the J and K inputs, as shown in the following logic table, during the Low-to-High clock transition. Clock transitions are ignored when CE is Low.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						**Outputs**
CLR	**PRE**	**CE**	**J**	**K**	**C**	**Q**
1	X	X	X	X	X	0
0	1	X	X	X	X	1
0	0	0	0	X	X	No Change
0	0	1	0	0	X	No Change
0	0	1	0	1	↑	0
0	0	1	1	0	↑	1
0	0	1	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

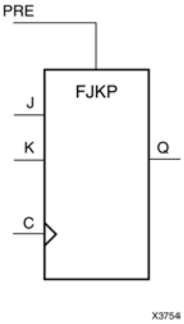
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FJKP

Macro: J-K Flip-Flop with Asynchronous Preset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single J-K-type flip-flop with J, K, and asynchronous preset (PRE) inputs and data output (Q). The asynchronous preset (PRE) input, when High, overrides all other inputs and sets the (Q) output High. When (PRE) is Low, the (Q) output responds to the state of the J and K inputs, as shown in the following logic table, during the Low-to-High clock transition.

For CPLD devices, this flip-flop is asynchronously cleared, output Low, when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				Outputs
PRE	**J**	**K**	**C**	**Q**
1	X	X	X	1
0	0	0	X	No Change
0	0	1	↑	0
0	1	0	↑	1
0	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

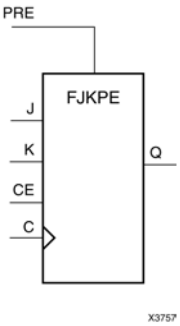
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration For Spartan®-6, Xilinx recommends that the INIT value always matches the polarity of the set or reset. For this element, the INIT should be 1. If set to 0, additional asynchronous circuitry will be created to correctly model the behavior.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FJKPE

Macro: J-K Flip-Flop with Clock Enable and Asynchronous Preset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single J-K-type flip-flop with J, K, clock enable (CE), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous preset (PRE), when High, overrides all other inputs and sets the (Q) output High. When (PRE) is Low and (CE) is High, the (Q) output responds to the state of the J and K inputs, as shown in the logic table, during the Low-to-High clock (C) transition. When (CE) is Low, clock transitions are ignored.

For CPLD devices, this flip-flop is asynchronously cleared, output Low, when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					Outputs
PRE	**CE**	**J**	**K**	**C**	**Q**
1	X	X	X	X	1
0	0	X	X	X	No Change
0	1	0	0	X	No Change
0	1	0	1	↑	0
0	1	1	0	↑	1
0	1	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

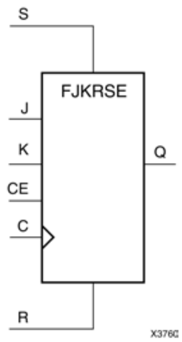
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration For Spartan®-6, Xilinx recommends that the INIT value always matches the polarity of the set or reset. For this element, the INIT should be 1. If set to 0, additional asynchronous circuitry will be created to correctly model the behavior.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FJKRSE

Macro: J-K Flip-Flop with Clock Enable and Synchronous Reset and Set



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single J-K-type flip-flop with J, K, synchronous reset (R), synchronous set (S), and clock enable (CE) inputs and data output (Q). When synchronous reset (R) is High during the Low-to-High clock (C) transition, all other inputs are ignored and output (Q) is reset Low. When synchronous set (S) is High and (R) is Low, output (Q) is set High. When (R) and (S) are Low and (CE) is High, output (Q) responds to the state of the J and K inputs, according to the following logic table, during the Low-to-High clock (C) transition. When (CE) is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs
R	**S**	**CE**	**J**	**K**	**C**	**Q**
1	X	X	X	X	↑	0
0	1	X	X	X	↑	1
0	0	0	X	X	X	No Change
0	0	1	0	0	X	No Change
0	0	1	0	1	↑	0
0	0	1	1	0	↑	1
0	0	1	1	0	↑	1
0	0	1	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

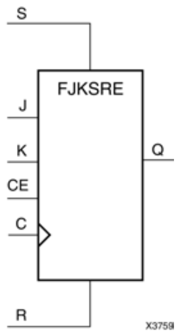
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FJKSRE

Macro: J-K Flip-Flop with Clock Enable and Synchronous Set and Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single J-K-type flip-flop with J, K, synchronous set (S), synchronous reset (R), and clock enable (CE) inputs and data output (Q). When synchronous set (S) is High during the Low-to-High clock (C) transition, all other inputs are ignored and output (Q) is set High. When synchronous reset (R) is High and (S) is Low, output (Q) is reset Low. When (S) and (R) are Low and (CE) is High, output (Q) responds to the state of the J and K inputs, as shown in the following logic table, during the Low-to-High clock (C) transition. When (CE) is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						**Outputs**
S	**R**	**CE**	**J**	**K**	**C**	**Q**
1	X	X	X	X	↑	1
0	1	X	X	X	↑	0
0	0	0	X	X	X	No Change
0	0	1	0	0	X	No Change
0	0	1	0	1	↑	0
0	0	1	1	0	↑	1
0	0	1	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

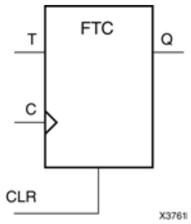
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FTC

Macro: Toggle Flip-Flop with Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a synchronous, resettable toggle flip-flop. The asynchronous clear (CLR) input, when High, overrides all other inputs and resets the data output (Q) Low. The (Q) output toggles, or changes state, when the toggle enable (T) input is High and (CLR) is Low during the Low-to-High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			Outputs
CLR	**T**	**C**	**Q**
1	X	X	0
0	0	X	No Change
0	1	↑	Toggle

Design Entry Method

You can instantiate this element when targeting a CPLD, but not when you are targeting an FPGA.

Available Attributes

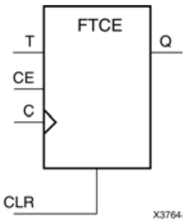
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration For Spartan®-6, the INIT value should always match the polarity of the set or reset. For this element, the INIT should be 0. If set to 1, an asynchronous circuit must be created to exhibit this behavior, which Xilinx does not recommend.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FTCE

Macro: Toggle Flip-Flop with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a toggle flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear (CLR) input is High, all other inputs are ignored and the data output (Q) is reset Low. When CLR is Low and toggle enable (T) and clock enable (CE) are High, Q output toggles, or changes state, during the Low-to-High clock (C) transition. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				Outputs
CLR	**CE**	**T**	**C**	**Q**
1	X	X	X	0
0	0	X	X	No Change
0	1	0	X	No Change
0	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

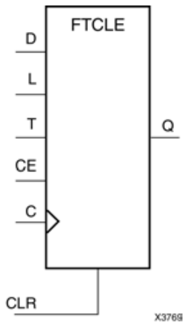
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration For Spartan®-6, the INIT value should always match the polarity of the set or reset. For this element, the INIT should be 0. If set to 1, an asynchronous circuit must be created to exhibit this behavior, which Xilinx does not recommend.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FTCLE

Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a toggle/loadable flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear input (CLR) is High, all other inputs are ignored and output Q is reset Low. When load enable input (L) is High and CLR is Low, clock enable (CE) is overridden and the data on data input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition. When toggle enable (T) and CE are High and L and CLR are Low, output Q toggles, or changes state, during the Low- to-High clock transition. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs
CLR	**L**	**CE**	**T**	**D**	**C**	**Q**
1	X	X	X	X	X	0
0	1	X	X	D	↑	D
0	0	0	X	X	X	No Change
0	0	1	0	X	X	No Change
0	0	1	1	X	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

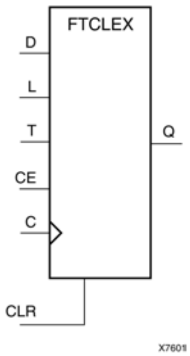
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration For Spartan®-6, the INIT value should always match the polarity of the set or reset. For this element, the INIT should be 0. If set to 1, an asynchronous circuit must be created to exhibit this behavior, which Xilinx does not recommend.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FTCLEX

Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a toggle/loadable flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear input (CLR) is High, all other inputs are ignored and output Q is reset Low. When load enable input (L) is High, CLR is Low, and CE is High, the data on data input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition. When toggle enable (T) and CE are High and L and CLR are Low, output Q toggles, or changes state, during the Low- to-High clock transition. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						**Outputs**
CLR	**L**	**CE**	**T**	**D**	**C**	**Q**
1	X	X	X	X	X	0
0	1	X	X	D	↑	D
0	0	0	X	X	X	No Change
0	0	1	0	X	X	No Change
0	0	1	1	X	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

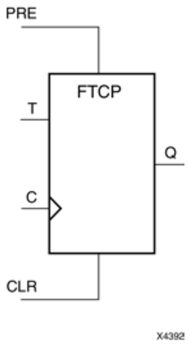
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration For Spartan®-6, the INIT value should always match the polarity of the set or reset. For this element, the INIT should be 0. If set to 1, an asynchronous circuit must be created to exhibit this behavior, which Xilinx does not recommend.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FTCP

Primitive: Toggle Flip-Flop with Asynchronous Clear and Preset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a toggle flip-flop with toggle enable and asynchronous clear and preset. When the asynchronous clear (CLR) input is High, all other inputs are ignored and the output (Q) is reset Low. When the asynchronous preset (PRE) is High and CLR is Low, all other inputs are ignored and Q is set High. When the toggle enable input (T) is High and CLR and PRE are Low, output Q toggles, or changes state, during the Low-to-High clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				**Outputs**
CLR	**PRE**	**T**	**C**	**Q**
1	X	X	X	0
0	1	X	X	1
0	0	0	X	No Change
0	0	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

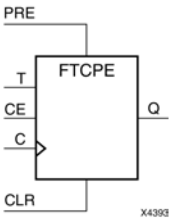
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FTCPE

Macro: Toggle Flip-Flop with Clock Enable and Asynchronous Clear and Preset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a toggle flip-flop with toggle and clock enable and asynchronous clear and preset. When the asynchronous clear (CLR) input is High, all other inputs are ignored and the output (Q) is reset Low. When the asynchronous preset (PRE) is High and CLR is Low, all other inputs are ignored and Q is set High. When the toggle enable input (T) and the clock enable input (CE) are High and CLR and PRE are Low, output Q toggles, or changes state, during the Low-to-High clock (C) transition. Clock transitions are ignored when CE is Low.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					Outputs
CLR	**PRE**	**CE**	**T**	**C**	**Q**
1	X	X	X	X	0
0	1	X	X	X	1
0	0	0	X	X	No Change
0	0	1	0	X	No Change
0	0	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

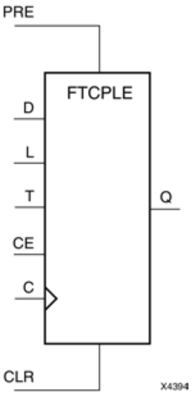
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FTCPLE

Macro: Loadable Toggle Flip-Flop with Clock Enable and Asynchronous Clear and Preset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a loadable toggle flip-flop with toggle and clock enable and asynchronous clear and preset. When the asynchronous clear (CLR) input is High, all other inputs are ignored and the output (Q) is reset Low. When the asynchronous preset (PRE) is High and CLR is Low, all other inputs are ignored and Q is set High. When the load input (L) is High, the clock enable input (CE) is overridden and data on data input (D) is loaded into the flip-flop during the Low-to-High clock transition. When the toggle enable input (T) and the clock enable input (CE) are High and CLR, PRE, and L are Low, output Q toggles, or changes state, during the Low-to-High clock (C) transition. Clock transitions are ignored when CE is Low.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs							**Outputs**
CLR	**PRE**	**L**	**CE**	**T**	**C**	**D**	**Q**
1	X	X	X	X	X	X	0
0	1	X	X	X	X	X	1
0	0	1	X	X	↑	0	0
0	0	1	X	X	↑	1	1
0	0	0	0	X	X	X	No Change
0	0	0	1	0	X	X	No Change
0	0	0	1	1	↑	X	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

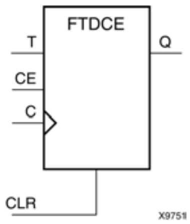
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FTDCE

Macro: Dual-Edge Triggered Toggle Flip-Flop with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a dual edge triggered toggle flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear (CLR) input is High, all other inputs are ignored and the data output (Q) is reset Low. When CLR is Low and toggle enable (T) and clock enable (CE) are High, Q output toggles, or changes state, during the Low-to-High and High-to-Low clock (C) transitions. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				**Outputs**
CLR	**CE**	**T**	**C**	**Q**
1	X	X	X	0
0	0	X	X	No Change
0	1	0	X	No Change
0	1	1	↑	Toggle
0	1	1	↓	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

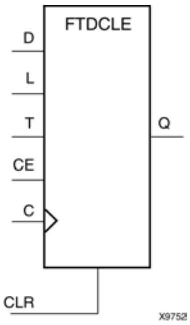
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FTDCLE

Macro: Dual-Edge Triggered Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a dual edge triggered toggle/loadable flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear input (CLR) is High, all other inputs are ignored and output Q is reset Low. When load enable input (L) is High and CLR is Low, clock enable (CE) is overridden and the data on data input (D) is loaded into the flip-flop during the Low-to-High and High-to-Low clock (C) transitions. When toggle enable (T) and CE are High and L and CLR are Low, output Q toggles, or changes state, during the Low- to-High and High-to-Low clock transitions. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs
CLR	**L**	**CE**	**T**	**D**	**C**	**Q**
1	X	X	X	X	X	0
0	1	X	X	1	↑	1
0	1	X	X	1	↓	1
0	1	X	X	0	↑	0
0	1	X	X	0	↓	0
0	0	0	X	X	X	No Change
0	0	1	0	X	X	No Change
0	0	1	1	X	↑	Toggle
0	0	1	1	X	↓	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

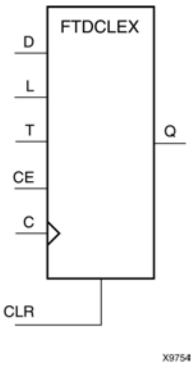
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FTDCLEX

Macro: Dual-Edge Triggered Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a dual edge triggered toggle/loadable flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear input (CLR) is High, all other inputs are ignored and output Q is reset Low. When load enable input (L) is High, CLR is Low, and CE is High, the data on data input (D) is loaded into the flip-flop during the Low-to-High and High-to-Low clock (C) transitions. When toggle enable (T) and CE are High and L and CLR are Low, output Q toggles, or changes state, during the Low- to-High and High-to-Low clock transitions. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						**Outputs**
CLR	**L**	**CE**	**T**	**D**	**C**	**Q**
1	X	X	X	X	X	0
0	1	1	X	1	↑	1
0	1	1	X	1	↓	1
0	1	1	X	0	↑	0
0	1	1	X	0	↓	0
0	0	0	X	X	X	No Change
0	0	1	0	X	X	No Change
0	0	1	1	X	↑	Toggle
0	0	1	1	X	↓	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

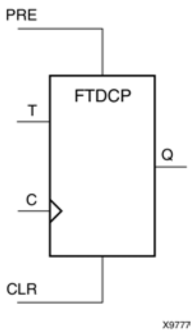
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FTDCP

Primitive: Dual-Edge Triggered Toggle Flip-Flop with Asynchronous Clear and Preset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a toggle flip-flop with toggle enable and asynchronous clear and preset. When the asynchronous clear (CLR) input is High, all other inputs are ignored and the output (Q) is reset Low. When the asynchronous preset (PRE) is High and CLR is Low, all other inputs are ignored and Q is set High. When the toggle enable input (T) is High and CLR and PRE are Low, output Q toggles, or changes state, during the Low-to-High and High-to-Low clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				Outputs
CLR	**PRE**	**T**	**C**	**Q**
1	X	X	X	0
0	1	X	X	1
0	0	0	X	No Change
0	0	1	↑	Toggle
0	0	1	↓	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

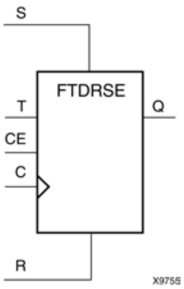
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FTDRSE

Macro: Dual-Edge Triggered Toggle Flip-Flop with Synchronous Reset, Set, and Clock Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a dual edge triggered toggle flip-flop with toggle and clock enable and synchronous reset and set. When the synchronous reset input (R) is High, it overrides all other inputs and the data output (Q) is reset Low. When the synchronous set input (S) is High and R is Low, clock enable input (CE) is overridden and output Q is set High. (Reset has precedence over Set.) When toggle enable input (T) and CE are High and R and S are Low, output Q toggles, or changes state, during the Low-to-High and High-to-Low clock transitions.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					Outputs
R	**S**	**CE**	**T**	**C**	**Q**
1	X	X	X	↑	0
1	X	X	X	↓	0
0	1	X	X	↑	1
0	1	X	X	↓	1
0	0	0	X	X	No Change
0	0	1	0	X	No Change
0	0	1	1	↑	Toggle
0	0	1	1	↓	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

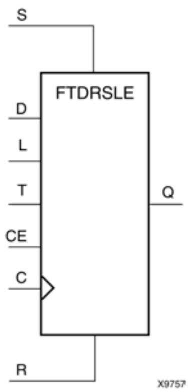
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FTDRSLE

Macro: Dual-Edge Triggered Toggle Flip-Flop with Clock Enable and Synchronous Reset and Set



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a dual edge triggered toggle/loadable flip-flop with toggle and clock enable and synchronous reset and set. The synchronous reset input (R), when High, overrides all other inputs and resets the data output (Q) Low. (Reset has precedence over Set.) When R is Low and synchronous set input (S) is High, the clock enable input (CE) is overridden and output Q is set High. When R and S are Low and load enable input (L) is High, CE is overridden and data on data input (D) is loaded into the flip-flop during the Low-to-High and High-to-Low clock transitions. When R, S, and L are Low and CE is High, output Q toggles, or changes state, during the Low-to-High and High-to-Low clock transitions. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs							Outputs
R	**S**	**L**	**CE**	**T**	**D**	**C**	**Q**
1	0	X	X	X	X	↑	0
1	0	X	X	X	X	↓	0
0	1	X	X	X	X	↑	1
0	1	X	X	X	X	↓	1
0	0	1	X	X	1	↑	1
0	0	1	X	X	1	↓	1
0	0	1	X	X	0	↑	0
0	0	1	X	X	0	↓	0
0	0	0	0	X	X	X	No Change
0	0	0	1	0	X	X	No Change
0	0	0	1	1	X	↑	Toggle
0	0	0	1	1	X	↓	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

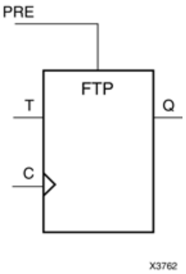
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FTP

Macro: Toggle Flip-Flop with Asynchronous Preset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a toggle flip-flop with toggle enable and asynchronous preset. When the asynchronous preset (PRE) input is High, all other inputs are ignored and output (Q) is set High. When toggle-enable input (T) is High and (PRE) is Low, output (Q) toggles, or changes state, during the Low-to-High clock (C) transition.

For CPLD devices, this flip-flop is asynchronously cleared, output Low, when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			**Outputs**
PRE	**T**	**C**	**Q**
1	X	X	1
0	0	X	No Change
0	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

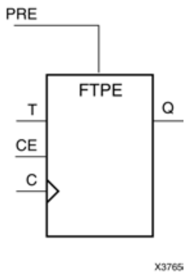
Attribute	**Type**	**Allowed Values**	**Default**	**Description**
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration For Spartan®-6, Xilinx recommends that the INIT value always matches the polarity of the set or reset. For this element, the INIT should be 1. If set to 0, additional asynchronous circuitry will be created to correctly model the behavior.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FTPE

Macro: Toggle Flip-Flop with Clock Enable and Asynchronous Preset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a toggle flip-flop with toggle and clock enable and asynchronous preset. When the asynchronous preset (PRE) input is High, all other inputs are ignored and output (Q) is set High. When the toggle enable input (T) is High, clock enable (CE) is High, and (PRE) is Low, output (Q) toggles, or changes state, during the Low-to-High clock transition. When (CE) is Low, clock transitions are ignored.

For CPLD devices, this flip-flop is asynchronously cleared, output Low, when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				Outputs
PRE	**CE**	**T**	**C**	**Q**
1	X	X	X	1
0	0	X	X	No Change
0	1	0	X	No Change
0	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

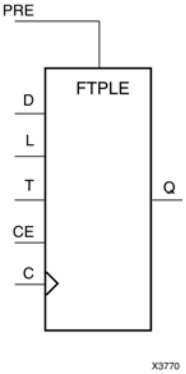
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration For Spartan®-6, Xilinx recommends that the INIT value always matches the polarity of the set or reset. For this element, the INIT should be 1. If set to 0, additional asynchronous circuitry will be created to correctly model the behavior.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FTPLE

Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Preset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a toggle/loadable flip-flop with toggle and clock enable and asynchronous preset. When the asynchronous preset input (PRE) is High, all other inputs are ignored and output (Q) is set High. When the load enable input (L) is High and (PRE) is Low, the clock enable (CE) is overridden and the data (D) is loaded into the flip-flop during the Low-to-High clock transition. When L and PRE are Low and toggle-enable input (T) and (CE) are High, output (Q) toggles, or changes state, during the Low-to-High clock transition. When (CE) is Low, clock transitions are ignored.

For CPLD devices, this flip-flop is asynchronously cleared, output Low, when power is applied. You can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs
PRE	**L**	**CE**	**T**	**D**	**C**	**Q**
1	X	X	X	X	X	1
0	1	X	X	D	↑	D
0	0	0	X	X	X	No Change
0	0	1	0	X	X	No Change
0	0	1	1	X	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

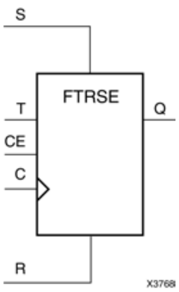
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration For Spartan®-6, Xilinx recommends that the INIT value always matches the polarity of the set or reset. For this element, the INIT should be 1. If set to 0, additional asynchronous circuitry will be created to correctly model the behavior.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FTRSE

Macro: Toggle Flip-Flop with Clock Enable and Synchronous Reset and Set



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a toggle flip-flop with toggle and clock enable and synchronous reset and set. When the synchronous reset input (R) is High, it overrides all other inputs and the data output (Q) is reset Low. When the synchronous set input (S) is High and (R) is Low, clock enable input (CE) is overridden and output (Q) is set High. (Reset has precedence over Set.) When toggle enable input (T) and (CE) are High and (R) and (S) are Low, output (Q) toggles, or changes state, during the Low-to-High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					Outputs
R	**S**	**CE**	**T**	**C**	**Q**
1	X	X	X	↑	0
0	1	X	X	↑	1
0	0	0	X	X	No Change
0	0	1	0	X	No Change
0	0	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

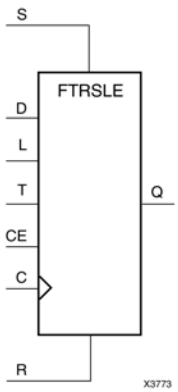
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FTRSLE

Macro: Toggle/Loadable Flip-Flop with Clock Enable and Synchronous Reset and Set



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a toggle/loadable flip-flop with toggle and clock enable and synchronous reset and set. The synchronous reset input (R), when High, overrides all other inputs and resets the data output (Q) Low. (Reset has precedence over Set.) When R is Low and synchronous set input (S) is High, the clock enable input (CE) is overridden and output Q is set High. When R and S are Low and load enable input (L) is High, CE is overridden and data on data input (D) is loaded into the flip-flop during the Low-to-High clock transition. When R, S, and L are Low, CE is High and T is High, output Q toggles, or changes state, during the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs							**Outputs**
R	**S**	**L**	**CE**	**T**	**D**	**C**	**Q**
1	0	X	X	X	X	↑	0
0	1	X	X	X	X	↑	1
0	0	1	X	X	1	↑	1
0	0	1	X	X	0	↑	0
0	0	0	0	X	X	X	No Change
0	0	0	1	0	X	X	No Change
0	0	0	1	1	X	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

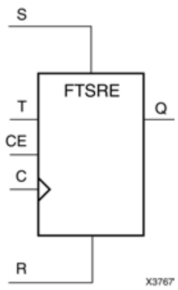
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FTSRE

Macro: Toggle Flip-Flop with Clock Enable and Synchronous Set and Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a toggle flip-flop with toggle and clock enable and synchronous set and reset. The synchronous set input, when High, overrides all other inputs and sets data output (Q) High. (Set has precedence over Reset.) When synchronous reset input (R) is High and S is Low, clock enable input (CE) is overridden and output Q is reset Low. When toggle enable input (T) and CE are High and S and R are Low, output Q toggles, or changes state, during the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs					**Outputs**
S	**R**	**CE**	**T**	**C**	**Q**
1	X	X	X	↑	1
0	1	X	X	↑	0
0	0	0	X	X	No Change
0	0	1	0	X	No Change
0	0	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

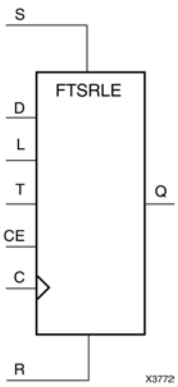
Attribute	**Type**	**Allowed Values**	**Default**	**Description**
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

FTSRLE

Macro: Toggle/Loadable Flip-Flop with Clock Enable and Synchronous Set and Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a toggle/loadable flip-flop with toggle and clock enable and synchronous set and reset. The synchronous set input (S), when High, overrides all other inputs and sets data output (Q) High. (Set has precedence over Reset.) When synchronous reset (R) is High and (S) is Low, clock enable input (CE) is overridden and output (Q) is reset Low. When load enable input (L) is High and S and R are Low, CE is overridden and data on data input (D) is loaded into the flip-flop during the Low-to-High clock transition. When the toggle enable input (T) and (CE) are High and (S), (R), and (L) are Low, output (Q) toggles, or changes state, during the Low-to-High clock transition. When (CE) is Low, clock transitions are ignored.

For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs							**Outputs**
S	**R**	**L**	**CE**	**T**	**D**	**C**	**Q**
1	X	X	X	X	X	↑	1
0	1	X	X	X	X	↑	0
0	0	1	X	X	1	↑	1
0	0	1	X	X	0	↑	0
0	0	0	0	X	X	X	No Change
0	0	0	1	0	X	X	No Change
0	0	0	1	1	X	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

GND

Primitive: Ground-Connection Signal Tag

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

The GND signal tag, or parameter, forces a net or input function to a Low logic level. A net tied to GND cannot have any other source.

When the logic-trimming software or fitter encounters a net or input function tied to GND, it removes any logic that is disabled by the GND signal. The GND signal is only implemented when the disabled logic cannot be removed.

Design Entry Method

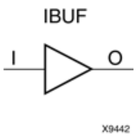
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

IBUF

Primitive: Input Buffer



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is automatically inserted (inferred) by the synthesis tool to any signal directly connected to a top-level input or in-out port of the design. You should generally let the synthesis tool infer this buffer. However, it can be instantiated into the design if required. In order to do so, connect the input port (I) directly to the associated top-level input or in-out port, and connect the output port (O) to the logic sourced by that port. Modify any necessary generic maps (VHDL) or named parameter value assignment (Verilog) in order to change the default behavior of the component.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Buffer output
I	Input	1	Buffer input

Design Entry Method

This design element can be used in schematics.

In general, this element is inferred by the synthesis tool for any specified top-level input port to the design. It is generally not necessary to specify them in the source code. However, if desired, they be manually instantiated by either copying the instantiation code from the appropriate Libraries Guide HDL template and pasting it into the top-level entity/module of your code. It is recommended to always put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level input port of the design and the O port to the logic in which this input is to source. Specify the desired generic/defparam values in order to configure the proper behavior of the buffer.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet.	"DEFAULT"	Assigns an I/O standard to the element.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- IBUF: Single-ended Input Buffer
--       All devices
-- Xilinx HDL Libraries Guide, version 11.2

IBUF_inst : IBUF
generic map (
   IBUF_DELAY_VALUE => "0", -- Specify the amount of added input delay for buffer,
                            -- "0"-"12" (Spartan-3E)
                            -- "0"-"16" (Spartan-3A)
   IFD_DELAY_VALUE => "AUTO", -- Specify the amount of added delay for input register,
                              -- "AUTO", "0"-"6" (Spartan-3E)
                              -- "AUTO", "0"-"8" (Spartan-3A)
   IOSTANDARD => "DEFAULT")
port map (
   O => O,     -- Buffer output
   I => I      -- Buffer input (connect directly to top-level port)
);

-- End of IBUF_inst instantiation
```

Verilog Instantiation Template

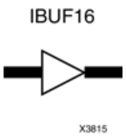
```
// IBUF: Single-ended Input Buffer
//       All devices
// Xilinx HDL Libraries Guide, version 11.2

IBUF #(
   .IBUF_DELAY_VALUE("0"),   // Specify the amount of added input delay for
                             //   the buffer: "0"-"12" (Spartan-3E)
                             //               "0"-"16" (Spartan-3A)
   .IFD_DELAY_VALUE("AUTO"), // Specify the amount of added delay for input
                             //   register: "AUTO", "0"-"6" (Spartan-3E)
                             //             "AUTO", "0"-"8" (Spartan-3A)
   .IOSTANDARD("DEFAULT")    // Specify the input I/O standard
)IBUF_inst (
   .O(O),     // Buffer output
   .I(I)      // Buffer input (connect directly to top-level port)
);

// End of IBUF_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate EDK documentation.

IBUF16

Macro: 16-Bit Input Buffer



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

Input Buffers isolate the internal circuit from the signals coming into the chip. This design element is contained in input/output blocks (IOBs) and allows the specification of the particular I/O Standard to configure the I/O. In general, an this element should be used for all single-ended data input or bidirectional pins.

Design Entry Method

This design element can be used in schematics.

In general, this element is inferred by the synthesis tool for any specified top-level input port to the design. It is generally not necessary to specify them in the source code. However, if desired, they be manually instantiated by either copying the instantiation code from the appropriate Libraries Guide HDL template and pasting it into the top-level entity/module of your code. It is recommended to always put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level input port of the design and the O port to the logic in which this input is to source. Specify the desired generic/defparam values in order to configure the proper behavior of the buffer.

Available Attributes

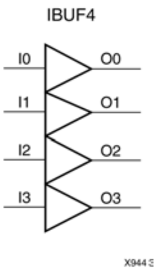
Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet.	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

IBUF4

Macro: 4-Bit Input Buffer



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

Input Buffers isolate the internal circuit from the signals coming into the chip. This design element is contained in input/output blocks (IOBs) and allows the specification of the particular I/O Standard to configure the I/O. In general, an this element should be used for all single-ended data input or bidirectional pins.

Design Entry Method

This design element can be used in schematics.

In general, this element is inferred by the synthesis tool for any specified top-level input port to the design. It is generally not necessary to specify them in the source code. However, if desired, they be manually instantiated by either copying the instantiation code from the appropriate Libraries Guide HDL template and pasting it into the top-level entity/module of your code. It is recommended to always put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level input port of the design and the O port to the logic in which this input is to source. Specify the desired generic/defparam values in order to configure the proper behavior of the buffer.

Available Attributes

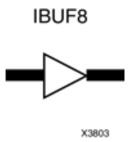
Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet.	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

IBUF8

Macro: 8-Bit Input Buffer



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

Input Buffers isolate the internal circuit from the signals coming into the chip. This design element is contained in input/output blocks (IOBs) and allows the specification of the particular I/O Standard to configure the I/O. In general, an this element should be used for all single-ended data input or bidirectional pins.

Design Entry Method

This design element can be used in schematics.

In general, this element is inferred by the synthesis tool for any specified top-level input port to the design. It is generally not necessary to specify them in the source code. However, if desired, they be manually instantiated by either copying the instantiation code from the appropriate Libraries Guide HDL template and pasting it into the top-level entity/module of your code. It is recommended to always put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level input port of the design and the O port to the logic in which this input is to source. Specify the desired generic/defparam values in order to configure the proper behavior of the buffer.

Available Attributes

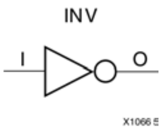
Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet.	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

INV

Primitive: Inverter



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single inverter that identifies signal inversions in a schematic.

Design Entry Method

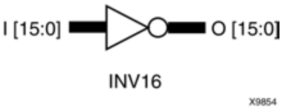
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

INV16

Macro: 16 Inverters



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a multiple inverter that identifies signal inversions in a schematic.

Design Entry Method

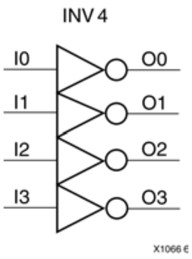
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

INV4

Macro: Four Inverters



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a multiple inverter that identifies signal inversions in a schematic.

Design Entry Method

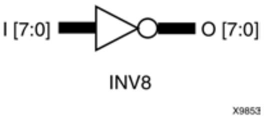
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

INV8

Macro: Eight Inverters



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a multiple inverter that identifies signal inversions in a schematic.

Design Entry Method

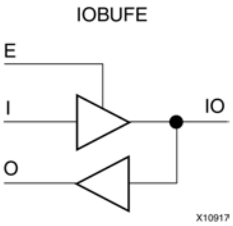
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

IOBUFE

Primitive: Bi-Directional Buffer



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a bi-directional buffer that is a composite of the IBUF and OBUFE elements. The O output is X (unknown) when IO (input/output) is Z. You can also implement IOBUFEs as interconnections of their component elements.

Logic Table

Inputs		Bidirectional	Outputs
E	**I**	**IO**	**O**
0	0	Z	X
0	1	Z	X
1	0	0	0
1	1	1	1

Design Entry Method

This design element is only for use in schematics.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- IOBUFE: Bi-Directional Buffer
--    XC9500XL/CoolRunner-II/XPLA-3
-- Xilinx HDL Language Template, version 10.1

IOBUFE_inst : IOBUFE
port map (O => user_O,
IO => user_IO,
I => user_I,
E => user_E);

-- End of IOBUFE_inst instantiation
```

Verilog Instantiation Template

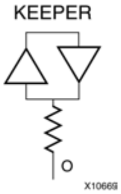
```
// IOBUFE: Bi-Directional Buffer
//    XC9500XL/CoolRunner-II/XPLA-3
// Xilinx HDL Language Template, version 10.1

IOBUFE IOBUFE_inst (.O (user_O),
.IO (user_IO),
.I (user_I),
.E (user_E));

// End of IOBUFE_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

KEEPER

Primitive: KEEPER Symbol



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

The design element is a weak keeper element that retains the value of the net connected to its bidirectional O pin. For example, if a logic 1 is being driven onto the net, KEEPER drives a weak/resistive 1 onto the net. If the net driver is then 3-stated, KEEPER continues to drive a weak/resistive 1 onto the net.

Port Descriptions

Name	Direction	Width	Function
O	Output	1-Bit	Keeper output

Design Entry Method

This design element can be used in schematics.

This element can be connected to a net in the following locations on a top-level schematic file:

- A net connected to an input IO Marker
- A net connected to both an output IO Marker and 3-statable IO element, such as an OBUFT.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- KEEPER: I/O Buffer Weak Keeper
--          All FPGA, CoolRunner-II
-- Xilinx HDL Libraries Guide, version 11.2

KEEPER_inst : KEEPER
port map (
   O => O     -- Keeper output (connect directly to top-level port)
);

-- End of KEEPER_inst instantiation
```

Verilog Instantiation Template

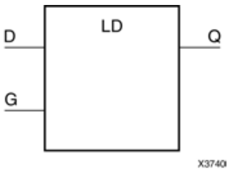
```
// KEEPER: I/O Buffer Weak Keeper
//         All FPGA, CoolRunner-II
// Xilinx HDL Libraries Guide, version 11.2

KEEPER KEEPER_inst (
   .O(O)     // Keeper output (connect directly to top-level port)
);

// End of KEEPER_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate EDK documentation.

LD

Primitive: Transparent Data Latch



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

LD is a transparent data latch. The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs		Outputs
G	**D**	**Q**
1	D	D
0	X	No Change
↓	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

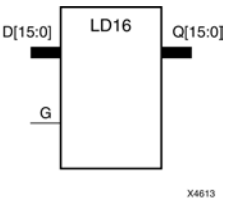
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

LD16

Macro: Multiple Transparent Data Latch



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element has 16 transparent data latches with a common gate enable (G). The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs		**Outputs**
G	**D**	**Q**
1	Dn	Dn
0	X	No Change
↓	Dn	Dn

Design Entry Method

This design element is only for use in schematics.

Available Attributes

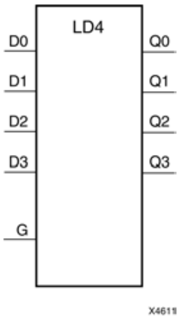
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	Any 16-Bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

LD4

Macro: Multiple Transparent Data Latch



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element has four transparent data latches with a common gate enable (G). The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs		**Outputs**
G	**D**	**Q**
1	Dn	Dn
0	X	No Change
↓	Dn	Dn

Design Entry Method

This design element is only for use in schematics.

Available Attributes

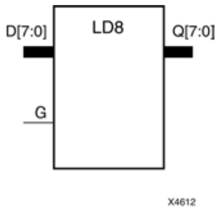
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	Any 4-Bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

LD8

Macro: Multiple Transparent Data Latch



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element has 8 transparent data latches with a common gate enable (G). The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs		Outputs
G	**D**	**Q**
1	Dn	Dn
0	X	No Change
↓	Dn	Dn

Design Entry Method

This design element is only for use in schematics.

Available Attributes

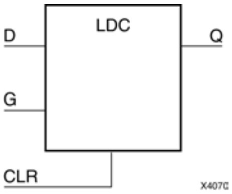
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	Any 8-Bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

LDC

Primitive: Macro: Transparent Data Latch with Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a transparent data latch with asynchronous clear. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) output Low. (Q) reflects the data (D) input while the gate enable (G) input is High and (CLR) is Low. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains low.

This latch is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs			Outputs
CLR	G	D	Q
1	X	X	0
0	1	D	D
0	0	X	No Change
0	↓	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

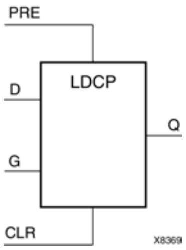
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

LDCP

Primitive: Transparent Data Latch with Asynchronous Clear and Preset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

The design element is a transparent data latch with data (D), asynchronous clear (CLR) and preset (PRE) inputs. When CLR is High, it overrides the other inputs and resets the data (Q) output Low. For XC9500 devices, when PRE is High and CLR is low, it presets the data (Q) output High. For CoolRunner™-II and CoolRunner™ XPLA3, PRE is a lower precedence than the gate (G) or data (D) inputs, and so has no influence on them. Q reflects the data (D) input while the gate (G) input is High and CLR and PRE are Low. The data on the D input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				Outputs
CLR	**PRE**	**G**	**D**	**Q**
1	X	X	X	0
0	X	1	X	1
0	0	1	D	D
0	0	0	X	No Change
0	0	↓	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

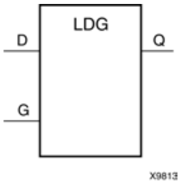
Attribute	Type	Allowed Values	Default	Description
INIT	Integer	0, 1	0	Specifies the initial value upon power-up or the assertion of GSR for the (Q) port.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

LDG

Primitive: Transparent Datagate Latch



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a transparent DataGate latch used for gating input signals to decrease power dissipation. The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is Low. The data on the D input during the Low-to-High gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains High.

The D input(s) of the LDG must be connected to a device input pad(s) and must have no other fan-outs (must not branch). The CPLD fitter maps the G input to the device's DataGate Enable control pin (DGE). There must be no more than one DataGate Enable signal in the design. The DataGate Enable signal may be driven either by a device input pin or any on-chip logic source. The DataGate Enable signal may be reused by other ordinary logic in the design.

This latch is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs		Outputs
G	**D**	**Q**
0	0	0
0	1	1
1	X	No Change
↑	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

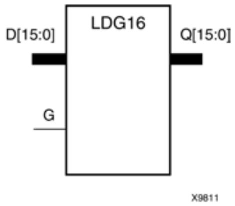
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

LDG16

Macro: 16-bit Transparent Datagate Latch



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element has 16 transparent DataGate latches with a common gate enable (G). These latches are used to gate input signals in order to decrease power dissipation during periods when activity on the input pins is not of interest to the CPLD. The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is Low. The data on the D input during the Low-to-High gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains High.

The D input(s) of the LDG must be connected to a device input pad(s) and must have no other fan-outs (must not branch). The CPLD fitter maps the G input to the device's DataGate Enable control pin (DGE). There must be no more than one DataGate Enable signal in the design. The DataGate Enable signal may be driven either by a device input pin or any on-chip logic source. The DataGate Enable signal may be reused by other ordinary logic in the design.

This latch is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs		Outputs
G	**D**	**Q**
0	0	0
0	1	1
1	X	No Change
↑	D	D

Design Entry Method

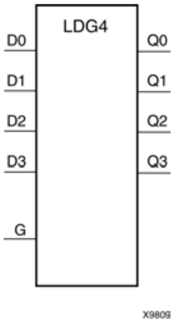
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

LDG4

Macro: 4-Bit Transparent Datagate Latch



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element has 4 transparent DataGate latches with a common gate enable (G). These latches are used to gate input signals in order to decrease power dissipation during periods when activity on the input pins is not of interest to the CPLD. The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is Low. The data on the D input during the Low-to-High gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains High.

The D input(s) of the LDG must be connected to a device input pad(s) and must have no other fan-outs (must not branch). The CPLD fitter maps the G input to the device's DataGate Enable control pin (DGE). There must be no more than one DataGate Enable signal in the design. The DataGate Enable signal may be driven either by a device input pin or any on-chip logic source. The DataGate Enable signal may be reused by other ordinary logic in the design.

This latch is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs		Outputs
G	**D**	**Q**
0	0	0
0	1	1
1	X	No Change
↑	D	D

Design Entry Method

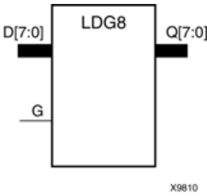
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

LDG8

Macro: 8-Bit Transparent Datagate Latch



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element has 8 transparent DataGate latches with a common gate enable (G). These latches are used to gate input signals in order to decrease power dissipation during periods when activity on the input pins is not of interest to the CPLD. The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is Low. The data on the D input during the Low-to-High gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains High.

The D input(s) of the LDG must be connected to a device input pad(s) and must have no other fan-outs (must not branch). The CPLD fitter maps the G input to the device's DataGate Enable control pin (DGE). There must be no more than one DataGate Enable signal in the design. The DataGate Enable signal may be driven either by a device input pin or any on-chip logic source. The DataGate Enable signal may be reused by other ordinary logic in the design.

This latch is asynchronously cleared, outputs Low, when power is applied. For CPLD devices, you can simulate power-on by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs		Outputs
G	**D**	**Q**
0	0	0
0	1	1
1	X	No Change
↑	D	D

Design Entry Method

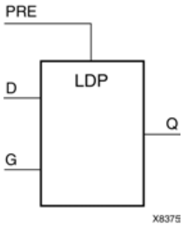
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

LDP

Primitive: Macro: Transparent Data Latch with Asynchronous Preset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a transparent data latch with asynchronous preset (PRE). For XC9500 devices, when PRE is High it overrides the other inputs and presets the data (Q) output High. For CoolRunner™-II and CoolRunner™ XPLA3, PRE is a lower precedence than the gate (G) or data (D) inputs, and so has no influence on them. Q reflects the data (D) input while gate (G) input is High and PRE is Low. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains Low.

The latch is asynchronously preset, output High, when power is applied.

Logic Table

Inputs			Outputs
PRE	**G**	**D**	**Q**
1	X	X	1
0	1	0	0
0	1	1	1
0	0	X	No Change
0	↓	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

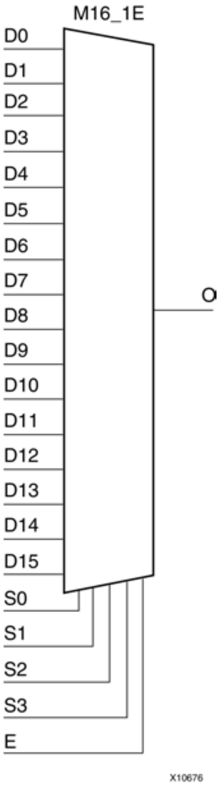
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Specifies the initial value upon power-up or the assertion of GSR for the Q port.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

M16_1E

Macro: 16-to-1 Multiplexer with Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 16-to-1 multiplexer with enable. When the enable input (E) is High, the M16_1E multiplexer chooses one data bit from 16 sources (D15 : D0) under the control of the select inputs (S3 : S0). The output (O) reflects the state of the selected input as shown in the logic table. When (E) is Low, the output is Low.

Logic Table

Inputs						Outputs
E	**S3**	**S2**	**S1**	**S0**	**D15-D0**	**O**
0	X	X	X	X	X	0
1	0	0	0	0	D0	D0
1	0	0	0	1	D1	D1
1	0	0	1	0	D2	D2
1	0	0	1	1	D3	D3
. . .	. . .	. . .	. . .	. . .	. . .	. . .
1	1	1	0	0	D12	D12
1	1	1	0	1	D13	D13
1	1	1	1	0	D14	D14
1	1	1	1	1	D15	D15

Design Entry Method

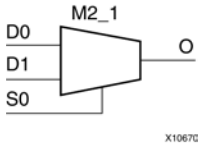
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

M2_1

Macro: 2-to-1 Multiplexer



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element chooses one data bit from two sources (D1 or D0) under the control of the select input (S0). The output (O) reflects the state of the selected data input. When Low, S0 selects D0 and when High, S0 selects D1.

Logic Table

Inputs			Outputs
S0	**D1**	**D0**	**O**
1	D1	X	D1
0	X	D0	D0

Design Entry Method

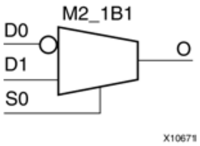
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

M2_1B1

Macro: 2-to-1 Multiplexer with D0 Inverted



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element chooses one data bit from two sources (D1 or D0) under the control of select input (S0). When S0 is Low, the output (O) reflects the inverted value of (D0). When S0 is High, (O) reflects the state of D1.

Logic Table

Inputs			Outputs
S0	**D1**	**D0**	**O**
1	1	X	1
1	0	X	0
0	X	1	0
0	X	0	1

Design Entry Method

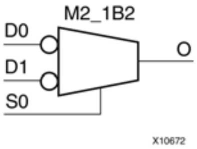
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

M2_1B2

Macro: 2-to-1 Multiplexer with D0 and D1 Inverted



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element chooses one data bit from two sources (D1 or D0) under the control of select input (S0). When S0 is Low, the output (O) reflects the inverted value of D0. When S0 is High, O reflects the inverted value of D1.

Logic Table

Inputs			Outputs
S0	**D1**	**D0**	**O**
1	1	X	0
1	0	X	1
0	X	1	0
0	X	0	1

Design Entry Method

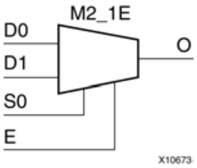
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

M2_1E

Macro: 2-to-1 Multiplexer with Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 2-to-1 multiplexer with enable. When the enable input (E) is High, the M2_1E chooses one data bit from two sources (D1 or D0) under the control of select input (S0). When Low, S0 selects D0 and when High, S0 selects D1. When (E) is Low, the output is Low.

Logic Table

Inputs				Outputs
E	**S0**	**D1**	**D0**	**O**
0	X	X	X	0
1	0	X	1	1
1	0	X	0	0
1	1	1	X	1
1	1	0	X	0

Design Entry Method

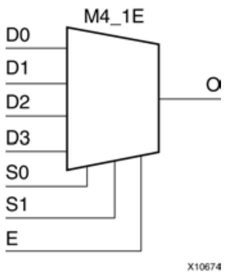
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

M4_1E

Macro: 4-to-1 Multiplexer with Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 4-to-1 multiplexer with enable. When the enable input (E) is High, the M4_1E multiplexer chooses one data bit from four sources (D3, D2, D1, or D0) under the control of the select inputs (S1 : S0). The output (O) reflects the state of the selected input as shown in the logic table. When (E) is Low, the output is Low.

Logic Table

Inputs							Outputs
E	**S1**	**S0**	**D0**	**D1**	**D2**	**D3**	**O**
0	X	X	X	X	X	X	0
1	0	0	D0	X	X	X	D0
1	0	1	X	D1	X	X	D1
1	1	0	X	X	D2	X	D2
1	1	1	X	X	X	D3	D3

Design Entry Method

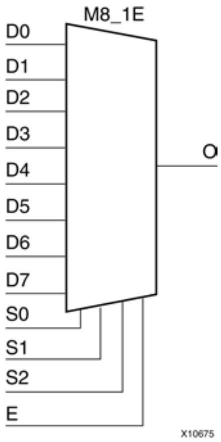
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

M8_1E

Macro: 8-to-1 Multiplexer with Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is an 8-to-1 multiplexer with enable. When the enable input (E) is High, the M8_1E multiplexer chooses one data bit from eight sources (D7 : D0) under the control of the select inputs (S2 : S0). The output (O) reflects the state of the selected input as shown in the logic table. When (E) is Low, the output is Low.

Logic Table

Inputs					Outputs
E	**S2**	**S1**	**S0**	**D7-D0**	**O**
0	X	X	X	X	0
1	0	0	0	D0	D0
1	0	0	1	D1	D1
1	0	1	0	D2	D2
1	0	1	1	D3	D3
1	1	0	0	D4	D4
1	1	0	1	D5	D5
1	1	1	0	D6	D6
1	1	1	1	D7	D7

Design Entry Method

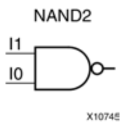
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NAND2

Primitive: 2-Input NAND Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

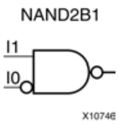
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NAND2B1

Primitive: 2-Input NAND Gate with 1 Inverted and 1 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

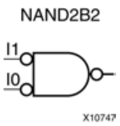
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NAND2B2

Primitive: 2-Input NAND Gate with Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

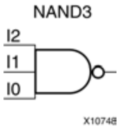
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NAND3

Primitive: 3-Input NAND Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

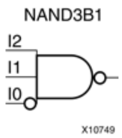
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NAND3B1

Primitive: 3-Input NAND Gate with 1 Inverted and 2 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

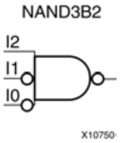
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NAND3B2

Primitive: 3-Input NAND Gate with 2 Inverted and 1 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

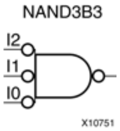
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NAND3B3

Primitive: 3-Input NAND Gate with Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

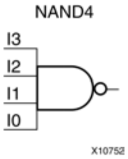
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NAND4

Primitive: 4-Input NAND Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

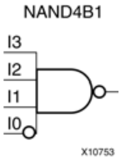
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NAND4B1

Primitive: 4-Input NAND Gate with 1 Inverted and 3 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

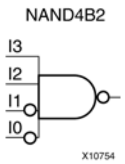
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NAND4B2

Primitive: 4-Input NAND Gate with 2 Inverted and 2 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

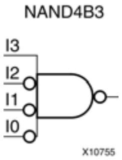
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NAND4B3

Primitive: 4-Input NAND Gate with 3 Inverted and 1 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

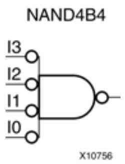
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NAND4B4

Primitive: 4-Input NAND Gate with Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

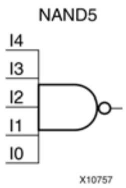
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NAND5

Primitive: 5-Input NAND Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

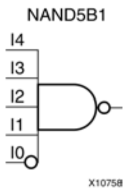
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NAND5B1

Primitive: 5-Input NAND Gate with 1 Inverted and 4 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

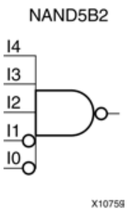
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NAND5B2

Primitive: 5-Input NAND Gate with 2 Inverted and 3 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

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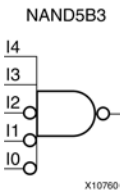
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NAND5B3

Primitive: 5-Input NAND Gate with 3 Inverted and 2 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

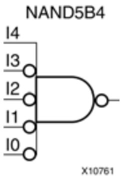
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NAND5B4

Primitive: 5-Input NAND Gate with 4 Inverted and 1 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

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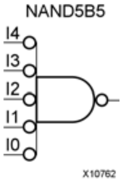
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NAND5B5

Primitive: 5-Input NAND Gate with Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

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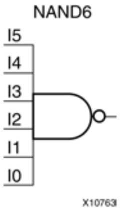
For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NAND6

Macro: 6-Input NAND Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

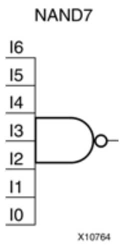
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NAND7

Macro: 7-Input NAND Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

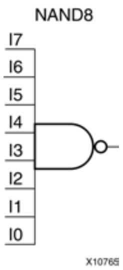
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NAND8

Macro: 8-Input NAND Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

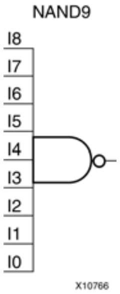
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NAND9

Macro: 9-Input NAND Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

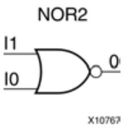
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NOR2

Primitive: 2-Input NOR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

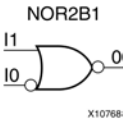
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NOR2B1

Primitive: 2-Input NOR Gate with 1 Inverted and 1 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

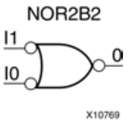
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NOR2B2

Primitive: 2-Input NOR Gate with Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

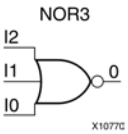
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NOR3

Primitive: 3-Input NOR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

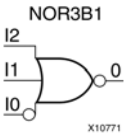
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NOR3B1

Primitive: 3-Input NOR Gate with 1 Inverted and 2 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

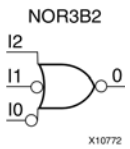
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NOR3B2

Primitive: 3-Input NOR Gate with 2 Inverted and 1 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

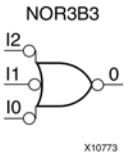
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NOR3B3

Primitive: 3-Input NOR Gate with Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

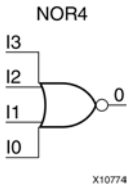
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NOR4

Primitive: 4-Input NOR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

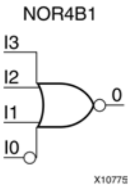
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NOR4B1

Primitive: 4-Input NOR Gate with 1 Inverted and 3 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

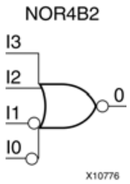
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NOR4B2

Primitive: 4-Input NOR Gate with 2 Inverted and 2 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

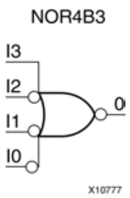
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NOR4B3

Primitive: 4-Input NOR Gate with 3 Inverted and 1 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

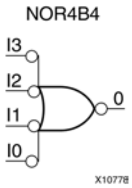
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NOR4B4

Primitive: 4-Input NOR Gate with Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

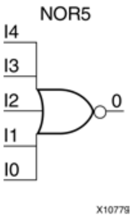
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NOR5

Primitive: 5-Input NOR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

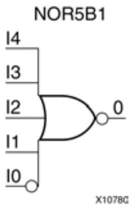
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NOR5B1

Primitive: 5-Input NOR Gate with 1 Inverted and 4 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

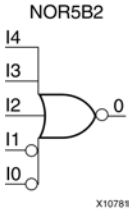
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NOR5B2

Primitive: 5-Input NOR Gate with 2 Inverted and 3 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

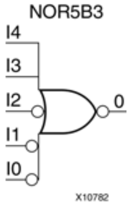
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NOR5B3

Primitive: 5-Input NOR Gate with 3 Inverted and 2 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

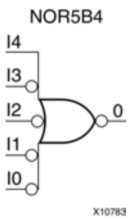
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NOR5B4

Primitive: 5-Input NOR Gate with 4 Inverted and 1 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

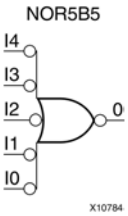
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NOR5B5

Primitive: 5-Input NOR Gate with Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

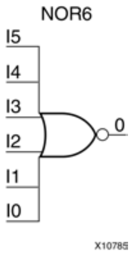
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NOR6

Macro: 6-Input NOR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

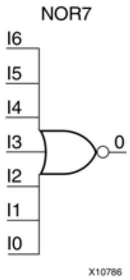
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NOR7

Macro: 7-Input NOR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

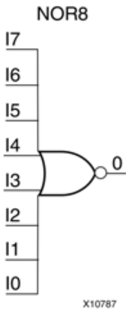
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NOR8

Macro: 8-Input NOR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

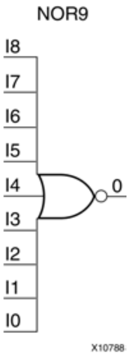
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

NOR9

Macro: 9-Input NOR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

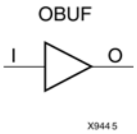
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OBUF

Primitive: Output Buffer



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a simple output buffer used to drive output signals to the FPGA device pins that do not need to be 3-stated (constantly driven). Either an OBUF, OBUFT, OBUFDS, or OBUFTDS must be connected to every output port in the design.

This element isolates the internal circuit and provides drive current for signals leaving a chip. It exists in input/output blocks (IOB). Its output (O) is connected to an OPAD or an IOPAD. The interface standard used by this element is LVTTL. Also, this element has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Output of OBUF to be connected directly to top-level output port.
I	Input	1	Input of OBUF. Connect to the logic driving the output port.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- OBUF: Single-ended Output Buffer
--       All devices
-- Xilinx HDL Libraries Guide, version 11.2

OBUF_inst : OBUF
generic map (
   DRIVE => 12,
   IOSTANDARD => "DEFAULT",
   SLEW => "SLOW")
port map (
   O => O,      -- Buffer output (connect directly to top-level port)
   I => I       -- Buffer input
);

-- End of OBUF_inst instantiation
```

Verilog Instantiation Template

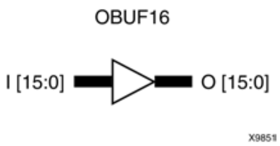
```
// OBUF: Single-ended Output Buffer
//       All devices
// Xilinx HDL Libraries Guide, version 11.2

OBUF #(
   .DRIVE(12),   // Specify the output drive strength
   .IOSTANDARD("DEFAULT"), // Specify the output I/O standard
   .SLEW("SLOW") // Specify the output slew rate
) OBUF_inst (
   .O(O),     // Buffer output (connect directly to top-level port)
   .I(I)      // Buffer input
);

// End of OBUF_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate EDK documentation.

OBUF16

Macro: 16-Bit Output Buffer



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a multiple output buffer.

This element isolates the internal circuit and provides drive current for signals leaving a chip. It exists in input/output blocks (IOB). Its output (O) is connected to an OPAD or an IOPAD. The interface standard used by this element is LVTTL. Also, this element has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

Design Entry Method

This design element can be used in schematics.

Available Attributes

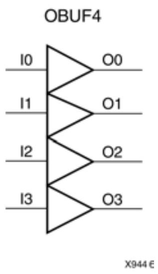
Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OBUF4

Macro: 4-Bit Output Buffer



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a multiple output buffer.

This element isolates the internal circuit and provides drive current for signals leaving a chip. It exists in input/output blocks (IOB). Its output (O) is connected to an OPAD or an IOPAD. The interface standard used by this element is LVTTL. Also, this element has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

Design Entry Method

This design element can be used in schematics.

Available Attributes

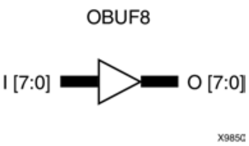
Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OBUF8

Macro: 8-Bit Output Buffer



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a multiple output buffer.

This element isolates the internal circuit and provides drive current for signals leaving a chip. It exists in input/output blocks (IOB). Its output (O) is connected to an OPAD or an IOPAD. The interface standard used by this element is LVTTL. Also, this element has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

Design Entry Method

This design element can be used in schematics.

Available Attributes

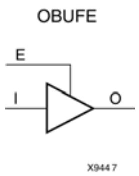
Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OBUFE

Macro: 3-State Output Buffer with Active-High Output Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 3-state buffer with input I, output O, and active-High output enable (E).

When E is High, data on the inputs of the buffers is transferred to the corresponding outputs. When E is Low, the output is High impedance (off or Z state). This design element isolates the internal circuit and provides drive current for signals leaving a chip. It is connected to an OPAD or an IOPAD, and its input is connected to the internal circuit.

Logic Table

Inputs		**Outputs**
E	**I**	**O**
0	X	Z
1	1	1
1	0	0

Design Entry Method

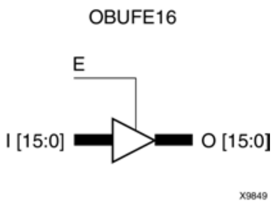
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OBUFE16

Macro: 16-Bit 3-State Output Buffer with Active-High Output Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 3-state buffer with input I15-I0, output O15-O0, and active-High output enable (E).

When E is High, data on the inputs of the buffers is transferred to the corresponding outputs. When E is Low, the output is High impedance (off or Z state). This design element isolates the internal circuit and provides drive current for signals leaving a chip. It is connected to an OPAD or an IOPAD, and its input is connected to the internal circuit.

Logic Table

Inputs		Outputs
E	**I**	**O**
0	X	Z
1	1	1
1	0	0

Design Entry Method

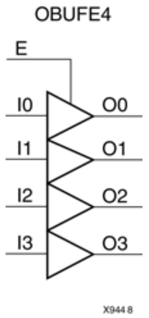
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OBUFE4

Macro: 4-Bit 3-State Output Buffer with Active-High Output Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 3-state buffer with input I3-I0, output O3-O0, and active-High output enable (E).

When E is High, data on the inputs of the buffers is transferred to the corresponding outputs. When E is Low, the output is High impedance (off or Z state). This design element isolates the internal circuit and provides drive current for signals leaving a chip. It is connected to an OPAD or an IOPAD, and its input is connected to the internal circuit.

Logic Table

Inputs		Outputs
E	**I**	**O**
0	X	Z
1	1	1
1	0	0

Design Entry Method

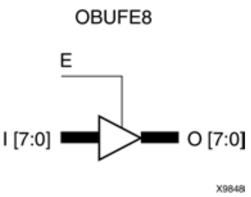
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OBUFE8

Macro: 8-Bit 3-State Output Buffer with Active-High Output Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a 3-state buffer with input I7-I0, output O7-O0, and active-High output enable (E).

When E is High, data on the inputs of the buffers is transferred to the corresponding outputs. When E is Low, the output is High impedance (off or Z state). This design element isolates the internal circuit and provides drive current for signals leaving a chip. It is connected to an OPAD or an IOPAD, and its input is connected to the internal circuit.

Logic Table

Inputs		Outputs
E	**I**	**O**
0	X	Z
1	1	1
1	0	0

Design Entry Method

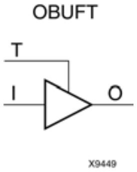
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OBUFT

Primitive: 3-State Output Buffer with Active Low Output Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a single, 3-state output buffer with input I, output O, and active-Low output enables (T). This element uses the LVTTL standard and has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (off or Z state). OBUFTs are generally used when a single-ended output is needed with a 3-state capability, such as the case when building bidirectional I/O.

Logic Table

Inputs		Outputs
T	**I**	**O**
1	X	Z
0	1	1
0	0	0

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Buffer output (connect directly to top-level port)
I	Input	1	Buffer input
T	Input	1	3-state enable input

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- OBUFT: Single-ended 3-state Output Buffer
--        All devices
-- Xilinx HDL Libraries Guide, version 11.2

OBUFT_inst : OBUFT
generic map (
   DRIVE => 12,
   IOSTANDARD => "DEFAULT",
   SLEW => "SLOW")
port map (
   O => O,     -- Buffer output (connect directly to top-level port)
   I => I,     -- Buffer input
   T => T      -- 3-state enable input
);

-- End of OBUFT_inst instantiation
```

Verilog Instantiation Template

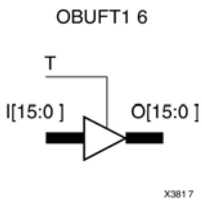
```
// OBUFT: Single-ended 3-state Output Buffer
//        All devices
// Xilinx HDL Libraries Guide, version 11.2

OBUFT #(
   .DRIVE(12),   // Specify the output drive strength
   .IOSTANDARD("DEFAULT"), // Specify the output I/O standard
   .SLEW("SLOW") // Specify the output slew rate
) OBUFT_inst (
   .O(O),     // Buffer output (connect directly to top-level port)
   .I(I),     // Buffer input
   .T(T)      // 3-state enable input
);

  // End of OBUFT_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate EDK documentation.

OBUFT16

Macro: 16-Bit 3-State Output Buffer with Active Low Output Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a multiple, 3-state output buffer with input I, output O, and active-Low output enables (T). This element uses the LVTTL standard and has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (off or Z state). OBUFTs are generally used when a single-ended output is needed with a 3-state capability, such as the case when building bidirectional I/O.

Logic Table

Inputs		Outputs
T	**I**	**O**
1	X	Z
0	1	1
0	0	0

Design Entry Method

This design element is only for use in schematics.

Available Attributes

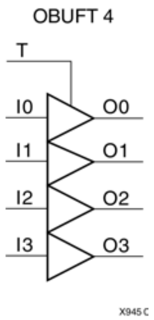
Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OBUFT4

Macro: 4-Bit 3-State Output Buffers with Active-Low Output Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a multiple, 3-state output buffer with input I, output O, and active-Low output enables (T). This element uses the LVTTL standard and has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (off or Z state). OBUFTs are generally used when a single-ended output is needed with a 3-state capability, such as the case when building bidirectional I/O.

Logic Table

Inputs		Outputs
T	**I**	**O**
1	X	Z
0	1	1
0	0	0

Design Entry Method

This design element is only for use in schematics.

Available Attributes

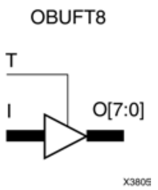
Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OBUFT8

Macro: 8-Bit 3-State Output Buffers with Active-Low Output Enable



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a multiple, 3-state output buffer with input I, output O, and active-Low output enables (T). This element uses the LVTTL standard and has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (off or Z state). OBUFTs are generally used when a single-ended output is needed with a 3-state capability, such as the case when building bidirectional I/O.

Logic Table

Inputs		Outputs
T	**I**	**O**
1	X	Z
0	1	1
0	0	0

Design Entry Method

This design element is only for use in schematics.

Available Attributes

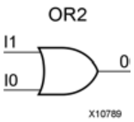
Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OR2

Primitive: 2-Input OR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

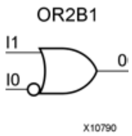
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OR2B1

Primitive: 2-Input OR Gate with 1 Inverted and 1 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

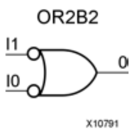
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OR2B2

Primitive: 2-Input OR Gate with Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

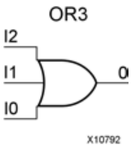
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OR3

Primitive: 3-Input OR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

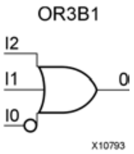
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OR3B1

Primitive: 3-Input OR Gate with 1 Inverted and 2 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

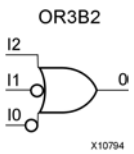
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OR3B2

Primitive: 3-Input OR Gate with 2 Inverted and 1 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

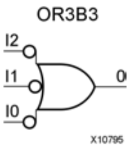
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OR3B3

Primitive: 3-Input OR Gate with Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

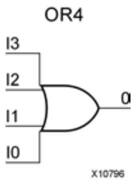
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OR4

Primitive: 4-Input OR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

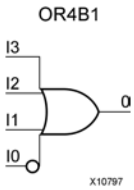
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OR4B1

Primitive: 4-Input OR Gate with 1 Inverted and 3 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

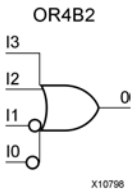
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OR4B2

Primitive: 4-Input OR Gate with 2 Inverted and 2 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

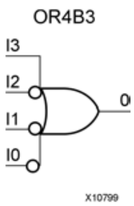
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OR4B3

Primitive: 4-Input OR Gate with 3 Inverted and 1 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

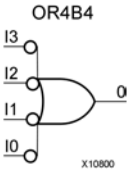
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OR4B4

Primitive: 4-Input OR Gate with Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

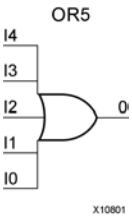
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OR5

Primitive: 5-Input OR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

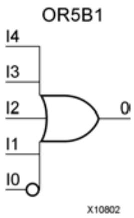
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OR5B1

Primitive: 5-Input OR Gate with 1 Inverted and 4 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

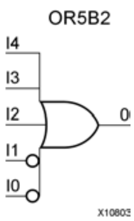
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OR5B2

Primitive: 5-Input OR Gate with 2 Inverted and 3 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

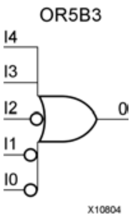
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OR5B3

Primitive: 5-Input OR Gate with 3 Inverted and 2 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

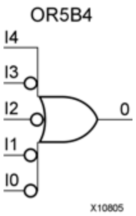
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OR5B4

Primitive: 5-Input OR Gate with 4 Inverted and 1 Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

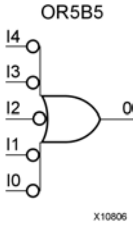
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OR5B5

Primitive: 5-Input OR Gate with Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

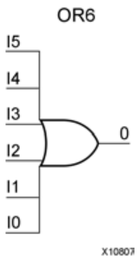
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OR6

Macro: 6-Input OR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

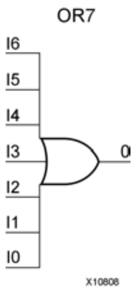
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OR7

Macro: 7-Input OR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

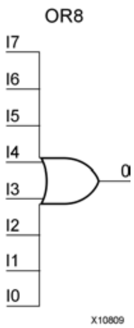
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OR8

Macro: 8-Input OR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

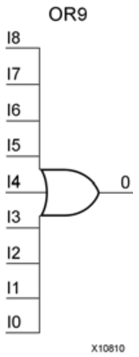
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

OR9

Macro: 9-Input OR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

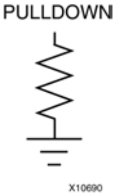
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

PULLDOWN

Primitive: Resistor to GND for Input Pads, Open-Drain, and 3-State Outputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This resistor element is connected to input, output, or bidirectional pads to guarantee a logic Low level for nodes that might float.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Pulldown output (connect directly to top level port)

Design Entry Method

This design element can be used in schematics.

This element can be connected to a net in the following locations on a top-level schematic file:

- A net connected to an input IO Marker.
- A net connected to both an output IO Marker and 3-statable IO element, such as an OBUFT.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- PULLDOWN: I/O Buffer Weak Pull-down
--          All FPGA
-- Xilinx HDL Libraries Guide, version 11.2

PULLDOWN_inst : PULLDOWN
port map (
   O => O     -- Pulldown output (connect directly to top-level port)
);

-- End of PULLDOWN_inst instantiation
```

Verilog Instantiation Template

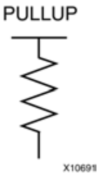
```
// PULLDOWN: I/O Buffer Weak Pull-down
//           All FPGA
// Xilinx HDL Libraries Guide, version 11.2

PULLDOWN PULLDOWN_inst (
   .O(O)     // Pulldown output (connect directly to top-level port)
);

// End of PULLDOWN_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate EDK documentation.

PULLUP

Primitive: Resistor to VCC for Input PADs, Open-Drain, and 3-State Outputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element allows for an input, 3-state output or bi-directional port to be driven to a weak high value when not being driven by an internal or external source. This element establishes a High logic level for open-drain elements and macros when all the drivers are off.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Pullup output (connect directly to top level port)

Design Entry Method

This design element can be used in schematics.

This element can be connected to a net in the following locations on a top-level schematic file:

- A net connected to an input IO Marker
- A net connected to both an output IO Marker and 3-statable IO element, such as an OBUFT.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;


-- PULLUP: I/O Buffer Weak Pull-up
--         All FPGA, CoolRunner-II
-- Xilinx HDL Libraries Guide, version 11.2

PULLUP_inst : PULLUP
port map (
   O => O     -- Pullup output (connect directly to top-level port)
);

-- End of PULLUP_inst instantiation
```

Verilog Instantiation Template

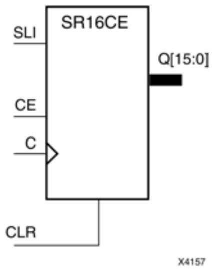
```
// PULLUP: I/O Buffer Weak Pull-up
//         All FPGA, CoolRunner-II
// Xilinx HDL Libraries Guide, version 11.2

PULLUP PULLUP_inst (
   .O(O)     // Pullup output (connect directly to top-level port)
);

// End of PULLUP_inst instantiation
```

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate EDK documentation.

SR16CE

Macro: 16-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel outputs (Q), and clock enable (CE) and asynchronous clear (CLR) inputs. The (CLR) input, when High, overrides all other inputs and resets the data outputs (Q) Low. When (CE) is High and (CLR) is Low, the data on the SLI input is loaded into the first bit of the shift register during the Low-to- High clock (C) transition and appears on the (Q0) output. During subsequent Low-to- High clock transitions, when (CE) is High and (CLR) is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (SLI→Q0, Q0→Q1, Q1→Q2, and so forth). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (CLR) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.

Logic Table

Inputs				Outputs	
CLR	**CE**	**SLI**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1
z = bit width - 1 qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

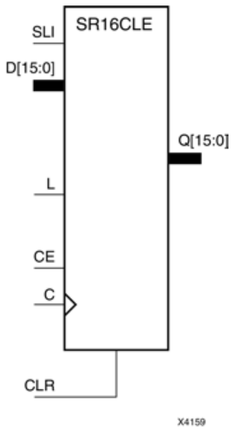
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SR16CLE

Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and asynchronous clear (CLR) . The register ignores clock transitions when (L) and (CE) are Low. The asynchronous (CLR), when High, overrides all other inputs and resets the data outputs (Q) Low. When (L) is High and (CLR) is Low, data on the Dn -D0 inputs is loaded into the corresponding Qn -(Q0) bits of the register.

When (CE) is High and (L) and (CLR) are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent clock transitions, when (CE) is High and (L) and (CLR) are Low, the data shifts to the next highest bit position as new data is loaded into (Q)0 (for example, SLI→Q0, Q0→Q1, and Q1→Q2).

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (CLR) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.

Logic Table

Inputs						Outputs	
CLR	L	CE	SLI	Dn : D0	C	Q0	Qz : Q1
1	X	X	X	X	X	0	0
0	1	X	X	Dn : D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1 qn-1 = state of referenced output one setup time prior to active clock transition							

Design Entry Method

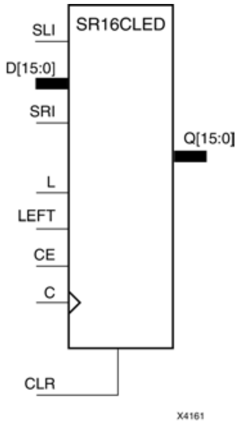
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SR16CLED

Macro: 16-Bit Shift Register with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs: clock enable (CE), load enable (L), shift left/right (LEFT), and asynchronous clear (CLR). The register ignores clock transitions when (CE) and (L) are Low. The asynchronous clear, when High, overrides all other inputs and resets the data outputs (Qn) Low.

When (L) is High and (CLR) is Low, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register. When (CE) is High and (L) and (CLR) are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on the SLI is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 or Q2) during subsequent clock transitions. If LEFT is Low, data on the SRI is loaded into the last (Q) output during the Low-to-High clock transition and shifted right during subsequent clock transitions. The logic tables indicate the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied.

Logic Table

Inputs								Outputs		
CLR	L	CE	LEFT	SLI	SRI	D15 : D0	C	Q0	Q15	Q14 : Q1
1	X	X	X	X	X	X	X	0	0	0
0	1	X	X	X	X	D15 : D0	↑	D0	D15	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q14	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1
qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition.										

Design Entry Method

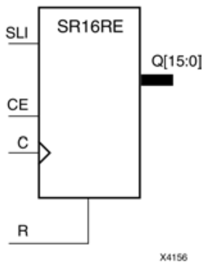
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SR16RE

Macro: 16-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with shift-left serial input (SLI), parallel outputs (Qn), clock enable (CE), and synchronous reset (R) inputs. The R input, when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low.

When (CE) is High and (R) is Low, the data on the (SLI) is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent Low-to-High clock transitions, when (CE) is High and R is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (for example, SLI→Q0, Q0→Q1, and Q1→Q2). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (R) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.

Logic Table

Inputs				Outputs	
R	**CE**	**SLI**	**C**	**Q0**	**Qz : Q1**
1	X	X	↑	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1
z = bitwidth -1 qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

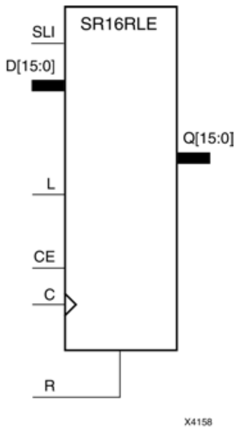
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SR16RLE

Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and synchronous reset (R). The register ignores clock transitions when (L) and (CE) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, data on the (D) inputs is loaded into the corresponding Q bits of the register.

When (CE) is High and (L) and (R) are Low, data on the (SLI) input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when (CE) is High and (L) and (R) are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (R) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.

Logic Table

Inputs						Outputs	
R	**L**	**CE**	**SLI**	**Dz : D0**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	X	↑	0	0
0	1	X	X	Dz : D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1 qn-1 = state of referenced output one setup time prior to active clock transition							

Design Entry Method

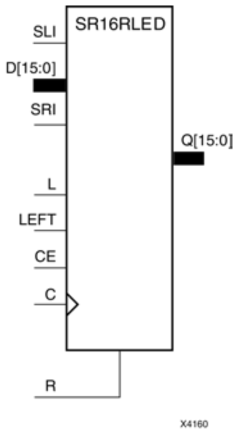
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SR16RLED

Macro: 16-Bit Shift Register with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q) and four control inputs — clock enable (CE), load enable (L), shift left/right (LEFT), and synchronous reset (R). The register ignores clock transitions when (CE) and (L) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register.

When (CE) is High and (L) and (R) are Low, data shifts right or left, depending on the state of the LEFT input. If LEFT is High, data on (SLI) is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 and Q2) during subsequent clock transitions. If LEFT is Low, data on the (SRI) is loaded into the last (Q) output during the Low-to-High clock transition and shifted right) during subsequent clock transitions. The logic tables below indicates the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied.

Logic Table

Inputs								Outputs		
R	L	CE	LEFT	SLI	SRI	D15:D0	C	Q0	Q15	Q14:Q1
1	X	X	X	X	X	X	↑	0	0	0
0	1	X	X	X	X	D15:D0	↓	D0	D15	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q14	qn-1
0	0	1	0	X	SRI	X	↓	q1	SRI	qn+1
qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition										

Design Entry Method

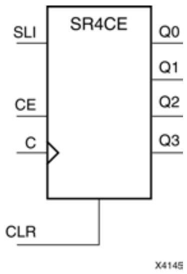
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SR4CE

Macro: 4-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel outputs (Q), and clock enable (CE) and asynchronous clear (CLR) inputs. The (CLR) input, when High, overrides all other inputs and resets the data outputs (Q) Low. When (CE) is High and (CLR) is Low, the data on the SLI input is loaded into the first bit of the shift register during the Low-to- High clock (C) transition and appears on the (Q0) output. During subsequent Low-to- High clock transitions, when (CE) is High and (CLR) is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (SLI→Q0, Q0→Q1, Q1→Q2, and so forth). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (CLR) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.

Logic Table

Inputs				Outputs	
CLR	**CE**	**SLI**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1
z = bit width - 1					
qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

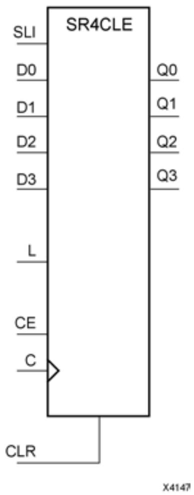
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SR4CLE

Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and asynchronous clear (CLR) . The register ignores clock transitions when (L) and (CE) are Low. The asynchronous (CLR), when High, overrides all other inputs and resets the data outputs (Q) Low. When (L) is High and (CLR) is Low, data on the Dn -D0 inputs is loaded into the corresponding Qn -(Q0) bits of the register.

When (CE) is High and (L) and (CLR) are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent clock transitions, when (CE) is High and (L) and (CLR) are Low, the data shifts to the next highest bit position as new data is loaded into (Q)0 (for example, SLI→Q0, Q0→Q1, and Q1→Q2).

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (CLR) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.

Logic Table

Inputs						Outputs	
CLR	**L**	**CE**	**SLI**	**Dn : D0**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	X	X	0	0
0	1	X	X	Dn : D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1							
qn-1 = state of referenced output one setup time prior to active clock transition							

Design Entry Method

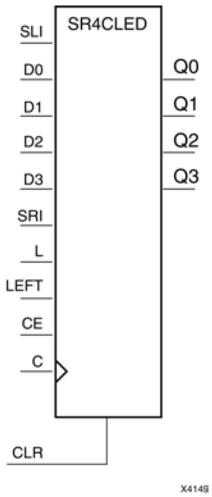
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SR4CLED

Macro: 4-Bit Shift Register with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs: clock enable (CE), load enable (L), shift left/right (LEFT), and asynchronous clear (CLR). The register ignores clock transitions when (CE) and (L) are Low. The asynchronous clear, when High, overrides all other inputs and resets the data outputs (Qn) Low.

When (L) is High and (CLR) is Low, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register. When (CE) is High and (L) and (CLR) are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on the SLI is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 or Q2) during subsequent clock transitions. If LEFT is Low, data on the SRI is loaded into the last (Q) output during the Low-to-High clock transition and shifted right during subsequent clock transitions. The logic tables indicate the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied.

Logic Table

Inputs								Outputs		
CLR	L	CE	LEFT	SLI	SRI	D3 : D0	C	Q0	Q3	Q2 : Q1
1	X	X	X	X	X	X	X	0	0	0
0	1	X	X	X	X	D3– D0	↑	D0	D3	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q2	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1
qn-1 and qn+1 = state of referenced output one setup time prior to active clock transition.										

Design Entry Method

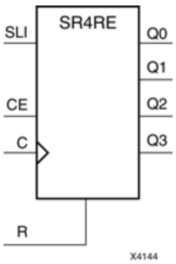
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SR4RE

Macro: 4-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with shift-left serial input (SLI), parallel outputs (Qn), clock enable (CE), and synchronous reset (R) inputs. The R input, when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low.

When (CE) is High and (R) is Low, the data on the (SLI) is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent Low-to-High clock transitions, when (CE) is High and R is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (for example, SLI→Q0, Q0→Q1, and Q1→Q2). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (R) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.

Logic Table

Inputs				**Outputs**	
R	**CE**	**SLI**	**C**	**Q0**	**Qz : Q1**
1	X	X	↑	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1
z = bitwidth -1 qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

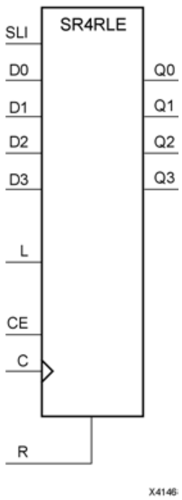
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SR4RLE

Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and synchronous reset (R). The register ignores clock transitions when (L) and (CE) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, data on the (D) inputs is loaded into the corresponding Q bits of the register.

When (CE) is High and (L) and (R) are Low, data on the (SLI) input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when (CE) is High and (L) and (R) are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (R) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.

Logic Table

Inputs						Outputs	
R	**L**	**CE**	**SLI**	**Dz : D0**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	X	↑	0	0
0	1	X	X	Dz : D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1 qn-1 = state of referenced output one setup time prior to active clock transition							

Design Entry Method

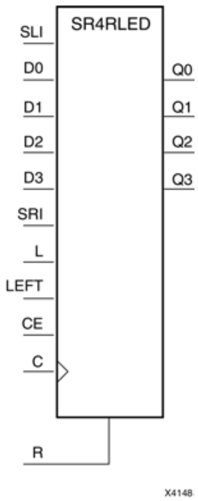
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SR4RLED

Macro: 4-Bit Shift Register with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q) and four control inputs — clock enable (CE), load enable (L), shift left/right (LEFT), and synchronous reset (R). The register ignores clock transitions when (CE) and (L) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register.

When (CE) is High and (L) and (R) are Low, data shifts right or left, depending on the state of the LEFT input. If LEFT is High, data on (SLI) is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 and Q2) during subsequent clock transitions. If LEFT is Low, data on the (SRI) is loaded into the last (Q) output during the Low-to-High clock transition and shifted right) during subsequent clock transitions. The logic tables below indicates the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied.

Logic Table

Inputs								Outputs		
R	**L**	**CE**	**LEFT**	**SLI**	**SRI**	**D3 : D0**	**C**	**Q0**	**Q3**	**Q2 : Q1**
1	X	X	X	X	X	X	↑	0	0	0
0	1	X	X	X	X	D3 : D0	↑	D0	D3	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q2	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1
qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition										

Design Entry Method

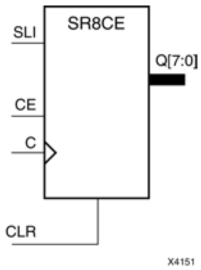
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SR8CE

Macro: 8-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel outputs (Q), and clock enable (CE) and asynchronous clear (CLR) inputs. The (CLR) input, when High, overrides all other inputs and resets the data outputs (Q) Low. When (CE) is High and (CLR) is Low, the data on the SLI input is loaded into the first bit of the shift register during the Low-to- High clock (C) transition and appears on the (Q0) output. During subsequent Low-to- High clock transitions, when (CE) is High and (CLR) is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (SLI→Q0, Q0→Q1, Q1→Q2, and so forth). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (CLR) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.

Logic Table

Inputs				**Outputs**	
CLR	**CE**	**SLI**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1
z = bit width - 1 qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

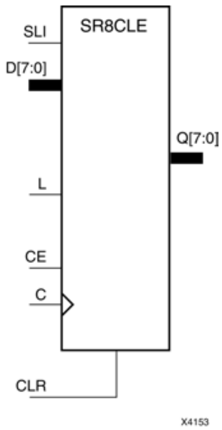
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SR8CLE

Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and asynchronous clear (CLR) . The register ignores clock transitions when (L) and (CE) are Low. The asynchronous (CLR), when High, overrides all other inputs and resets the data outputs (Q) Low. When (L) is High and (CLR) is Low, data on the Dn -D0 inputs is loaded into the corresponding Qn -(Q0) bits of the register.

When (CE) is High and (L) and (CLR) are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent clock transitions, when (CE) is High and (L) and (CLR) are Low, the data shifts to the next highest bit position as new data is loaded into (Q)0 (for example, SLI→Q0, Q0→Q1, and Q1→Q2).

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (CLR) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.

Logic Table

Inputs						Outputs	
CLR	**L**	**CE**	**SLI**	**Dn : D0**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	X	X	0	0
0	1	X	X	Dn : D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1							
qn-1 = state of referenced output one setup time prior to active clock transition							

Design Entry Method

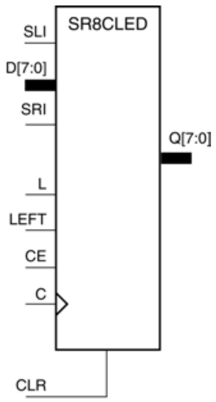
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SR8CLED

Macro: 8-Bit Shift Register with Clock Enable and Asynchronous Clear



X4155

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs: clock enable (CE), load enable (L), shift left/right (LEFT), and asynchronous clear (CLR). The register ignores clock transitions when (CE) and (L) are Low. The asynchronous clear, when High, overrides all other inputs and resets the data outputs (Qn) Low.

When (L) is High and (CLR) is Low, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register. When (CE) is High and (L) and (CLR) are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on the SLI is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 or Q2) during subsequent clock transitions. If LEFT is Low, data on the SRI is loaded into the last (Q) output during the Low-to-High clock transition and shifted right during subsequent clock transitions. The logic tables indicate the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied.

Logic Table

Inputs								Outputs		
CLR	**L**	**CE**	**LEFT**	**SLI**	**SRI**	**D7 : D0**	**C**	**Q0**	**Q7**	**Q6 : Q1**
1	X	X	X	X	X	X	X	0	0	0
0	1	X	X	X	X	D7 : D0	↑	D0	D7	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q6	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1
qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition.										

Design Entry Method

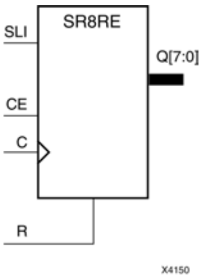
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SR8RE

Macro: 8-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with shift-left serial input (SLI), parallel outputs (Qn), clock enable (CE), and synchronous reset (R) inputs. The R input, when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low.

When (CE) is High and (R) is Low, the data on the (SLI) is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent Low-to-High clock transitions, when (CE) is High and R is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (for example, SLI→Q0, Q0→Q1, and Q1→Q2). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (R) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.

Logic Table

Inputs				Outputs	
R	**CE**	**SLI**	**C**	**Q0**	**Qz : Q1**
1	X	X	↑	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1
z = bitwidth -1 qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

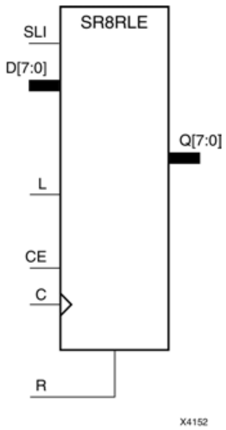
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SR8RLE

Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and synchronous reset (R). The register ignores clock transitions when (L) and (CE) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, data on the (D) inputs is loaded into the corresponding Q bits of the register.

When (CE) is High and (L) and (R) are Low, data on the (SLI) input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when (CE) is High and (L) and (R) are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (R) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.

Logic Table

Inputs						Outputs	
R	**L**	**CE**	**SLI**	**Dz : D0**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	X	↑	0	0
0	1	X	X	Dz : D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1							
qn-1 = state of referenced output one setup time prior to active clock transition							

Design Entry Method

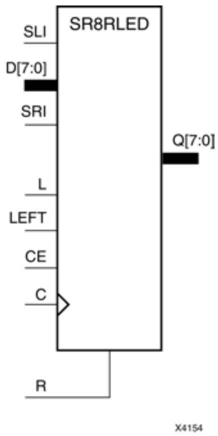
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SR8RLED

Macro: 8-Bit Shift Register with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q) and four control inputs — clock enable (CE), load enable (L), shift left/right (LEFT), and synchronous reset (R). The register ignores clock transitions when (CE) and (L) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register.

When (CE) is High and (L) and (R) are Low, data shifts right or left, depending on the state of the LEFT input. If LEFT is High, data on (SLI) is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 and Q2) during subsequent clock transitions. If LEFT is Low, data on the (SRI) is loaded into the last (Q) output during the Low-to-High clock transition and shifted right) during subsequent clock transitions. The logic tables below indicates the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied.

Logic Table

Inputs								Outputs		
R	**L**	**CE**	**LEFT**	**SLI**	**SRI**	**D7 : D0**	**C**	**Q0**	**Q7**	**Q6 : Q1**
1	X	X	X	X	X	X	↑	0	0	0
0	1	X	X	X	X	D7 : D0	↓	D0	D7	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q6	qn-1
0	0	1	0	X	SRI	X	↓	q1	SRI	qn+1
qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition										

Design Entry Method

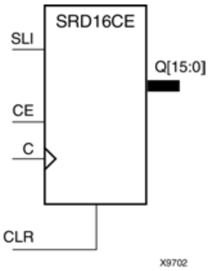
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SRD16CE

Macro: 16-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with a shift-left serial input (SLI), parallel outputs (Q), clock enable (CE) and asynchronous clear (CLR) inputs. The CLR input, when High, overrides all other inputs and resets the data outputs (Q) Low. When CE is High and CLR is Low, the data on the SLI input is loaded into the first bit of the shift register during the Low-to-High (or High-to-Low) clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and CLR is Low, data shifts to the next highest bit position as new data is loaded into Q0. The register ignores clock transitions when CE is Low.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, CE, and CLR in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.

The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				**Outputs**	
CLR	**CE**	**SLI**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	0	0
0	0	X	X	No Change	No Change
0	1	1	↑	1	qn-1
0	1	1	↓	1	qn-1
0	1	0	↑	0	qn-1
0	1	0	↓	0	qn-1
z = bitwidth -1					
qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

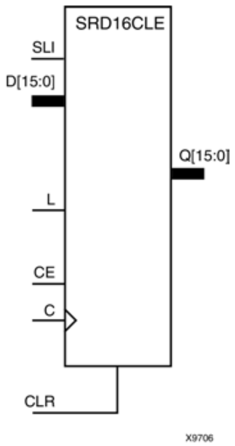
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SRD16CLE

Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with a shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and asynchronous clear (CLR). The register ignores clock transitions when L and CE are Low. The asynchronous CLR, when High, overrides all other inputs and resets the data outputs (Q) Low. When L is High and CLR is Low, data on the Dn:D0 inputs is loaded into the corresponding Qn:Q0 bits of the register. When CE is High and L and CLR are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High (or High-to-Low) clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and L and CLR are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, CE, L, and CLR inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs	
CLR	L	CE	SLI	Dn:D0	C	Q0	Qz:Q1
1	X	X	X	X	X	0	0
0	1	X	X	Dn:D0	↑	D0	Dn
0	1	X	X	Dn:D0	↓	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	1	SLI	X	↓	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1 qn-1 = state of referenced output one setup time prior to active clock transition							

Design Entry Method

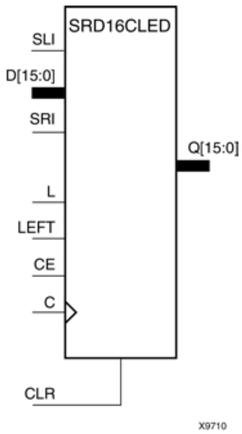
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SRD16CLED

Macro: 16-Bit Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs: clock enable (CE), load enable (L), shift left/right (LEFT), and asynchronous clear (CLR). The register ignores clock transitions when CE and L are Low. The asynchronous clear, when High, overrides all other inputs and resets the data outputs (Qn) Low. When L is High and CLR is Low, the data on the D inputs is loaded into the corresponding Q bits of the register. When CE is High and L and CLR are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on the SLI is loaded into Q0 during the Low-to-High or High-to-Low clock transition and shifted left during subsequent clock transitions. If LEFT is Low, data on the SRI is loaded into the last Q output during the Low-to-High or High-to-Low clock transition and shifted right during subsequent clock transitions. The logic table indicates the state of the Q outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs								Outputs		
CLR	**L**	**CE**	**LEFT**	**SLI**	**SRI**	**D15 : D0**	**C**	**Q0**	**Q15**	**Q14 : Q1**
1	X	X	X	X	X	X	X	0	0	0
0	1	X	X	X	X	D15 : D0	↑	D0	D15	Dn
0	1	X	X	X	X	D15 : D0	↓	D0	D15	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q14	qn-1
0	0	1	1	SLI	X	X	↓	SLI	q14	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1
0	0	1	0	X	SRI	X	↓	q1	SRI	qn+1
qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition.										

Design Entry Method

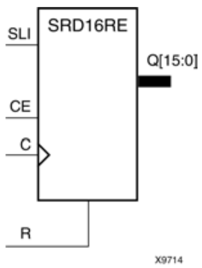
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SRD16RE

Macro: 16-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with shift-left serial input (SLI), parallel outputs (Qn), clock enable (CE), and synchronous reset (R) inputs. The R input, when High, overrides all other inputs during the Low-to-High or High-to-Low clock (C) transition and resets the data outputs (Q) Low. When CE is High and R is Low, the data on the SLI is loaded into the first bit of the shift register during the Low-to-High clock or High-to-Low (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and R is Low, data shifts to the next highest bit position as new data is loaded into Q0. The register ignores clock transitions when CE is Low.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, CE, and R in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				Outputs	
R	**CE**	**SLI**	**C**	**Q0**	**Qz:Q1**
1	X	X	↑	0	0
1	X	X	↓	0	0
0	0	X	X	No Change	No Change
0	1	1	↑	1	qn-1
0	1	1	↓	1	qn-1
0	1	0	↑	0	qn-1
0	1	0	↓	0	qn-1

z = bitwidth -1

qn-1 = state of referenced output one setup time prior to active clock transition

Design Entry Method

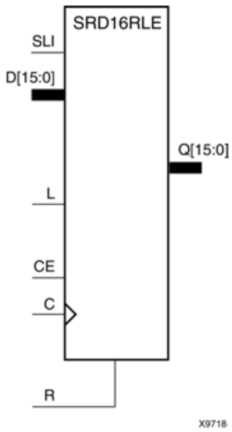
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SRD16RLE

Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and synchronous reset (R). The register ignores clock transitions when L and CE are Low. The synchronous R, when High, overrides all other inputs during the Low-to-High or High-to-Low clock (C) transition and resets the data outputs (Q) Low. When L is High and R is Low, data on the D inputs is loaded into the corresponding Q bits of the register. When CE is High and L and R are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High or High-to-Low clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and L and R are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, CE, L, and R inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs	
R	**L**	**CE**	**SLI**	**Dz:D0**	**C**	**Q0**	**Qz:Q1**
1	X	X	X	X	↑	0	0
1	X	X	X	X	↓	0	0
0	1	X	X	Dz:D0	↑	D0	Dn
0	1	X	X	Dz:D0	↓	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	1	SLI	X	↓	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1							

Design Entry Method

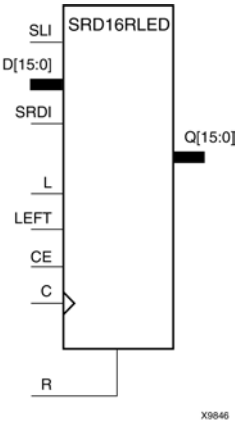
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SRD16RLED

Macro: 16-Bit Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with shift-left (SLI) and shift-right (SRDI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs — clock enable (CE), load enable (L), shift left/right (LEFT), and synchronous reset (R). The register ignores clock transitions when CE and L are Low. The synchronous R, when High, overrides all other inputs during the Low-to-High or High-to-Low clock (C) transition and resets the data outputs (Q) Low. When L is High and R is Low, the data on the D inputs is loaded into the corresponding Q bits of the register. When CE is High and L and R are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on SLI is loaded into Q0 during the Low-to-High or High-to-Low clock transition and shifted left (to Q1, Q2, etc.) during subsequent clock transitions. If LEFT is Low, data on the SRDI is loaded into the last Q output during the Low-to-High or High-to-Low clock transition and shifted right during subsequent clock transitions. The logic table indicates the state of the Q outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs								Outputs		
R	L	CE	LEFT	SLI	SRDI	D15 : D0	C	Q0	Q15	Q14 : Q1
1	X	X	X	X	X	X	↑	0	0	0
1	X	X	X	X	X	X	↓	0	0	0
0	1	X	X	X	X	D15 : D0	↑	D0	D15	Dn
0	1	X	X	X	X	D15 : D0	↓	D0	D15	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q14	qn-1
0	0	1	1	SLI	X	X	↓	SLI	q14	qn-1
0	0	1	0	X	SRDI	X	↑	q1	SRDI	qn+1
0	0	1	0	X	SRDI	X	↓	q1	SRDI	qn+1
qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition										

Design Entry Method

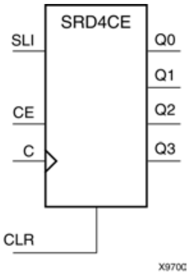
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SRD4CE

Macro: 4-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with a shift-left serial input (SLI), parallel outputs (Q), clock enable (CE) and asynchronous clear (CLR) inputs. The CLR input, when High, overrides all other inputs and resets the data outputs (Q) Low. When CE is High and CLR is Low, the data on the SLI input is loaded into the first bit of the shift register during the Low-to-High (or High-to-Low) clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and CLR is Low, data shifts to the next highest bit position as new data is loaded into Q0. The register ignores clock transitions when CE is Low.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, CE, and CLR in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.

The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				**Outputs**	
CLR	**CE**	**SLI**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	0	0
0	0	X	X	No Change	No Change
0	1	1	↑	1	qn-1
0	1	1	↓	1	qn-1
0	1	0	↑	0	qn-1
0	1	0	↓	0	qn-1
z = bitwidth -1					
qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

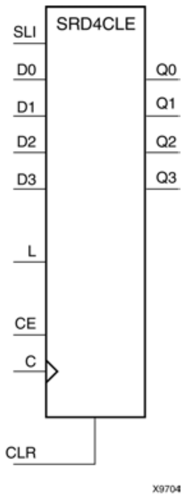
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SRD4CLE

Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with a shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and asynchronous clear (CLR). The register ignores clock transitions when L and CE are Low. The asynchronous CLR, when High, overrides all other inputs and resets the data outputs (Q) Low. When L is High and CLR is Low, data on the Dn:D0 inputs is loaded into the corresponding Qn:Q0 bits of the register. When CE is High and L and CLR are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High (or High-to-Low) clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and L and CLR are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, CE, L, and CLR inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs	
CLR	**L**	**CE**	**SLI**	**Dn:D0**	**C**	**Q0**	**Qz:Q1**
1	X	X	X	X	X	0	0
0	1	X	X	Dn:D0	↑	D0	Dn
0	1	X	X	Dn:D0	↓	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	1	SLI	X	↓	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1							
qn-1 = state of referenced output one setup time prior to active clock transition							

Design Entry Method

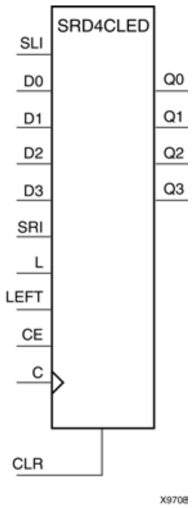
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SRD4CLED

Macro: 4-Bit Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs: clock enable (CE), load enable (L), shift left/right (LEFT), and asynchronous clear (CLR). The register ignores clock transitions when CE and L are Low. The asynchronous clear, when High, overrides all other inputs and resets the data outputs (Qn) Low. When L is High and CLR is Low, the data on the D inputs is loaded into the corresponding Q bits of the register. When CE is High and L and CLR are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on the SLI is loaded into Q0 during the Low-to-High or High-to-Low clock transition and shifted left during subsequent clock transitions. If LEFT is Low, data on the SRI is loaded into the last Q output during the Low-to-High or High-to-Low clock transition and shifted right during subsequent clock transitions. The logic table indicates the state of the Q outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs								Outputs		
CLR	L	CE	LEFT	SLI	SRI	D3:D0	C	Q0	Q3	Q2:Q1
1	X	X	X	X	X	X	X	0	0	0
0	1	X	X	X	X	D3:D0	↑	D0	D3	Dn
0	1	X	X	X	X	D3:D0	↓	D0	D3	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q2	qn-1
0	0	1	1	SLI	X	X	↓	SLI	q2	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1
0	0	1	0	X	SRI	X	↓	q1	SRI	qn+1
qn-1 and qn+1 = state of referenced output one setup time prior to active clock transition										

Design Entry Method

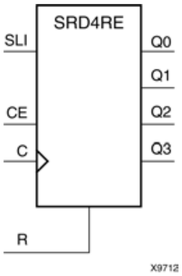
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SRD4RE

Macro: 4-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with shift-left serial input (SLI), parallel outputs (Qn), clock enable (CE), and synchronous reset (R) inputs. The R input, when High, overrides all other inputs during the Low-to-High or High-to-Low clock (C) transition and resets the data outputs (Q) Low. When CE is High and R is Low, the data on the SLI is loaded into the first bit of the shift register during the Low-to-High clock or High-to-Low (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and R is Low, data shifts to the next highest bit position as new data is loaded into Q0. The register ignores clock transitions when CE is Low.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, CE, and R in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				Outputs	
R	**CE**	**SLI**	**C**	**Q0**	**Qz:Q1**
1	X	X	↑	0	0
1	X	X	↓	0	0
0	0	X	X	No Change	No Change
0	1	1	↑	1	qn-1
0	1	1	↓	1	qn-1
0	1	0	↑	0	qn-1
0	1	0	↓	0	qn-1
z = bitwidth -1 qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

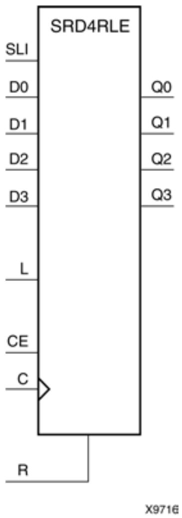
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SRD4RLE

Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and synchronous reset (R). The register ignores clock transitions when L and CE are Low. The synchronous R, when High, overrides all other inputs during the Low-to-High or High-to-Low clock (C) transition and resets the data outputs (Q) Low. When L is High and R is Low, data on the D inputs is loaded into the corresponding Q bits of the register. When CE is High and L and R are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High or High-to-Low clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and L and R are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, CE, L, and R inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs	
R	**L**	**CE**	**SLI**	**Dz:D0**	**C**	**Q0**	**Qz:Q1**
1	X	X	X	X	↑	0	0
1	X	X	X	X	↓	0	0
0	1	X	X	Dz:D0	↑	D0	Dn
0	1	X	X	Dz:D0	↓	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	1	SLI	X	↓	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1							

Design Entry Method

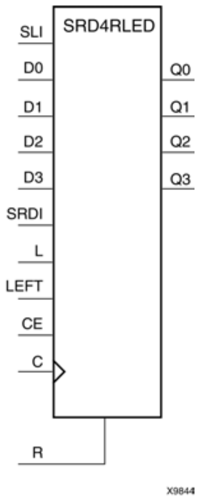
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SRD4RLED

Macro: 4-Bit Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with shift-left (SLI) and shift-right (SRDI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs — clock enable (CE), load enable (L), shift left/right (LEFT), and synchronous reset (R). The register ignores clock transitions when CE and L are Low. The synchronous R, when High, overrides all other inputs during the Low-to-High or High-to-Low clock (C) transition and resets the data outputs (Q) Low. When L is High and R is Low, the data on the D inputs is loaded into the corresponding Q bits of the register. When CE is High and L and R are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on SLI is loaded into Q0 during the Low-to-High or High-to-Low clock transition and shifted left (to Q1, Q2, etc.) during subsequent clock transitions. If LEFT is Low, data on the SRDI is loaded into the last Q output during the Low-to-High or High-to-Low clock transition and shifted right during subsequent clock transitions. The logic table indicates the state of the Q outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs								Outputs		
R	L	CE	LEFT	SLI	SRDI	D3:D0	C	Q0	Q3	Q2:Q1
1	X	X	X	X	X	X↑	↑	0	0	0
1	X	X	X	X	X	X	↓	0	0	0
0	1	X	X	X	X	D3 : D0	↑	D0	D3	Dn
0	1	X	X	X	X	D3 : D0	↓	D0	D3	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q2	qn-1
0	0	1	1	SLI	X	X	↓	SLI	q2	qn-1
0	0	1	0	X	SRDI	X	↑	q1	SRDI	qn+1
0	0	1	0	X	SRDI	X	↓	q1	SRDI	qn+1
qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition										

Design Entry Method

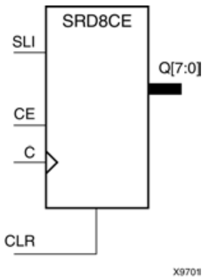
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SRD8CE

Macro: 8-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with a shift-left serial input (SLI), parallel outputs (Q), clock enable (CE) and asynchronous clear (CLR) inputs. The CLR input, when High, overrides all other inputs and resets the data outputs (Q) Low. When CE is High and CLR is Low, the data on the SLI input is loaded into the first bit of the shift register during the Low-to-High (or High-to-Low) clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and CLR is Low, data shifts to the next highest bit position as new data is loaded into Q0. The register ignores clock transitions when CE is Low.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, CE, and CLR in parallel.

This register is asynchronously cleared, outputs Low, when power is applied.

The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				**Outputs**	
CLR	**CE**	**SLI**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	0	0
0	0	X	X	No Change	No Change
0	1	1	↑	1	qn-1
0	1	1	↓	1	qn-1
0	1	0	↑	0	qn-1
0	1	0	↓	0	qn-1
z = bitwidth -1					
qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

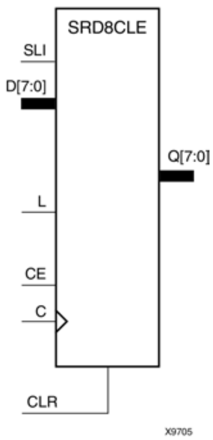
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SRD8CLE

Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with a shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and asynchronous clear (CLR). The register ignores clock transitions when L and CE are Low. The asynchronous CLR, when High, overrides all other inputs and resets the data outputs (Q) Low. When L is High and CLR is Low, data on the Dn:D0 inputs is loaded into the corresponding Qn:Q0 bits of the register. When CE is High and L and CLR are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High (or High-to-Low) clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and L and CLR are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, CE, L, and CLR inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs	
CLR	**L**	**CE**	**SLI**	**Dn:D0**	**C**	**Q0**	**Qz:Q1**
1	X	X	X	X	X	0	0
0	1	X	X	Dn:D0	↑	D0	Dn
0	1	X	X	Dn:D0	↓	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	1	SLI	X	↓	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1 qn-1 = state of referenced output one setup time prior to active clock transition							

Design Entry Method

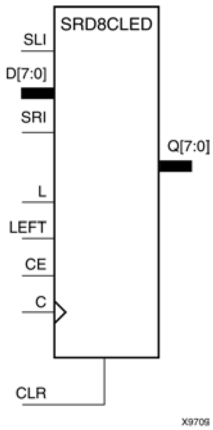
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SRD8CLED

Macro: 8-Bit Dual Edge Triggered Shift Register with Clock Enable and Asynchronous Clear



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs: clock enable (CE), load enable (L), shift left/right (LEFT), and asynchronous clear (CLR). The register ignores clock transitions when CE and L are Low. The asynchronous clear, when High, overrides all other inputs and resets the data outputs (Qn) Low. When L is High and CLR is Low, the data on the D inputs is loaded into the corresponding Q bits of the register. When CE is High and L and CLR are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on the SLI is loaded into Q0 during the Low-to-High or High-to-Low clock transition and shifted left during subsequent clock transitions. If LEFT is Low, data on the SRI is loaded into the last Q output during the Low-to-High or High-to-Low clock transition and shifted right during subsequent clock transitions. The logic table indicates the state of the Q outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs								Outputs		
CLR	L	CE	LEFT	SLI	SRI	D7:D0	C	Q0	Q7	Q6:Q1
1	X	X	X	X	X	X	X	0	0	0
0	1	X	X	X	X	D7:D0	↑	D0	D7	Dn
0	1	X	X	X	X	D7:D0	↓	D0	D7	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q6	qn-1
0	0	1	1	SLI	X	X	↓	SLI	q6	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1
0	0	1	0	X	SRI	X	↓	q1	SRI	qn+1
qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition										

Design Entry Method

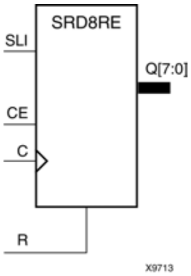
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SRD8RE

Macro: 8-Bit Serial-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with shift-left serial input (SLI), parallel outputs (Qn), clock enable (CE), and synchronous reset (R) inputs. The R input, when High, overrides all other inputs during the Low-to-High or High-to-Low clock (C) transition and resets the data outputs (Q) Low. When CE is High and R is Low, the data on the SLI is loaded into the first bit of the shift register during the Low-to-High clock or High-to-Low (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and R is Low, data shifts to the next highest bit position as new data is loaded into Q0. The register ignores clock transitions when CE is Low.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, CE, and R in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs				**Outputs**	
R	**CE**	**SLI**	**C**	**Q0**	**Qz:Q1**
1	X	X	↑	0	0
1	X	X	↓	0	0
0	0	X	X	No Change	No Change
0	1	1	↑	1	qn-1
0	1	1	↓	1	qn-1
0	1	0	↑	0	qn-1
0	1	0	↓	0	qn-1
z = bitwidth -1					
qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

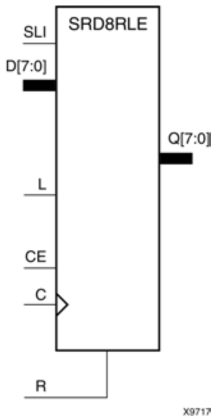
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SRD8RLE

Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and synchronous reset (R). The register ignores clock transitions when L and CE are Low. The synchronous R, when High, overrides all other inputs during the Low-to-High or High-to-Low clock (C) transition and resets the data outputs (Q) Low. When L is High and R is Low, data on the D inputs is loaded into the corresponding Q bits of the register. When CE is High and L and R are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High or High-to-Low clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when CE is High and L and R are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, CE, L, and R inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs						Outputs	
R	**L**	**CE**	**SLI**	**Dz:D0**	**C**	**Q0**	**Qz:Q1**
1	X	X	X	X	↑	0	0
1	X	X	X	X	↓	0	0
0	1	X	X	Dz:D0	↑	D0	Dn
0	1	X	X	Dz:D0	↓	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	1	SLI	X	↓	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1							

Design Entry Method

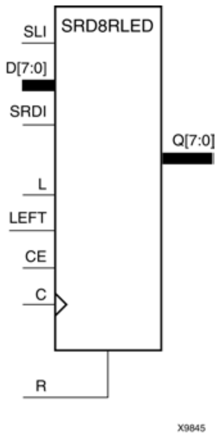
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

SRD8RLED

Macro: 8-Bit Dual Edge Triggered Shift Register with Clock Enable and Synchronous Reset



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II

Introduction

This design element is a dual edge triggered shift register with shift-left (SLI) and shift-right (SRDI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs — clock enable (CE), load enable (L), shift left/right (LEFT), and synchronous reset (R). The register ignores clock transitions when CE and L are Low. The synchronous R, when High, overrides all other inputs during the Low-to-High or High-to-Low clock (C) transition and resets the data outputs (Q) Low. When L is High and R is Low, the data on the D inputs is loaded into the corresponding Q bits of the register. When CE is High and L and R are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on SLI is loaded into Q0 during the Low-to-High or High-to-Low clock transition and shifted left (to Q1, Q2, etc.) during subsequent clock transitions. If LEFT is Low, data on the SRDI is loaded into the last Q output during the Low-to-High or High-to-Low clock transition and shifted right during subsequent clock transitions. The logic table indicates the state of the Q outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. The power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Logic Table

Inputs								Outputs		
R	**L**	**CE**	**LEFT**	**SLI**	**SRDI**	**D7 : D0**	**C**	**Q0**	**Q7**	**Q6 : Q1**
1	X	X	X	X	X	X	↑	0	0	0
1	X	X	X	X	X	X	↓	0	0	0
0	1	X	X	X	X	D7 : D0	↑	D0	D7	Dn
0	1	X	X	X	X	D7 : D0	↓	D0	D7	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q6	qn-1
0	0	1	1	SLI	X	X	↓	SLI	q6	qn-1
0	0	1	0	X	SRDI	X	↑	q1	SRDI	qn+1
0	0	1	0	X	SRDI	X	↓	q1	SRDI	qn+1
qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition										

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

VCC

Primitive: VCC-Connection Signal Tag

Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

This design element serves as a signal tag, or parameter, that forces a net or input function to a logic High level. A net tied to this element cannot have any other source.

When the placement and routing software encounters a net or input function tied to this element, it removes any logic that is disabled by the Vcc signal, which is only implemented when the disabled logic cannot be removed.

Design Entry Method

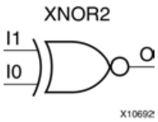
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

XNOR2

Primitive: 2-Input XNOR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

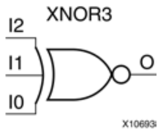
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

XNOR3

Primitive: 3-Input XNOR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

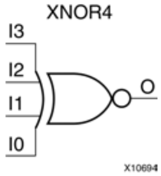
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

XNOR4

Primitive: 4-Input XNOR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

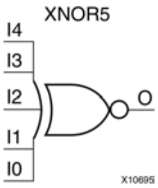
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

XNOR5

Primitive: 5-Input XNOR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

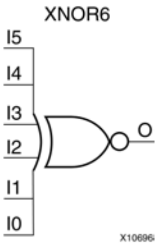
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

XNOR6

Macro: 6-Input XNOR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

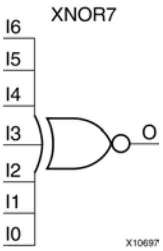
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

XNOR7

Macro: 7-Input XNOR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

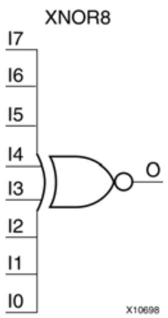
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

XNOR8

Macro: 8-Input XNOR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

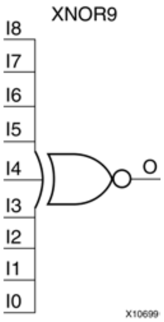
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

XNOR9

Macro: 9-Input XNOR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

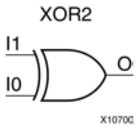
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

XOR2

Primitive: 2-Input XOR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

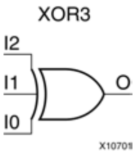
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

XOR3

Primitive: 3-Input XOR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

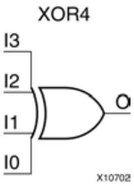
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

XOR4

Primitive: 4-Input XOR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

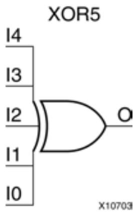
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

XOR5

Primitive: 5-Input XOR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

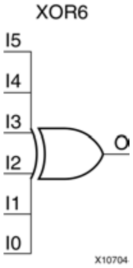
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

XOR6

Macro: 6-Input XOR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

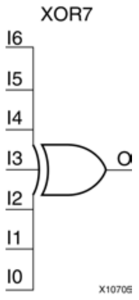
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

XOR7

Macro: 7-Input XOR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

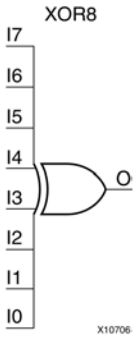
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

XOR8

Macro: 8-Input XOR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

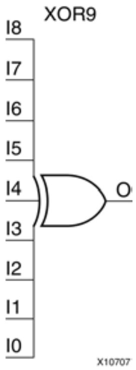
This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.

XOR9

Macro: 9-Input XOR Gate with Non-Inverted Inputs



Supported Architectures

This design element is supported in the following architectures:

- XC9500
- CoolRunner™-II
- CoolRunner XPLA3

Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the appropriate CPLD User Guide.
- See the appropriate CPLD Data Sheets.